Extended Abstracts of the 2000 International Conference on Solid State Devices and Materials, Sendai, 2000, pp. 474–475

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Design of SiGe/Buried Oxide Layered Structure to Form Highly Strained Si Layer on Insulator for SOI MOSFETs

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1. Introduction

We have proposed and demonstrated advanced SOI MOSFETs with strained Si channel, which is epitaxially grown on SiGe / buried insulator layered structure using the SIMOX process and regrowth technique [1.2]. Since larger strain in the strained-Si channel leads to higher mobility, thin and relaxed SiGe layer on buried oxide with higher Ge content is strongly required for the MOSFETs with higher current drive. In this paper, we present two ideas for the appropriate design of the SiGe / buried oxide layered structure. First, diffusion of Ge atoms during the high temperature annealing in the SIMOX process is studied, and the importance of the design of the structure before SIMOX process considering the diffusion is addressed. Next, a novel SiGe-on-insulator structure including the growth of SiGe with higher Ge content layer on lower Ge content, which acts as the dislocation absorber, is proposed and the effectiveness of this structure is expeimentally verified.

2. Ge diffusion during the annealing

Two samples are prepared for evaluating the Ge diffusion during the SIMOX annealing,. The sample A has a 1 μm thick $Si_{0.9}Ge_{0.1}$ layer on a Si (100) substrate inserting the graded Ge composition layer. In the sample B, a 0.5 μm $Si_{0.9}Ge_{0.1}$ layer is directly grown on the substrate (see fig. 1). Each sample is annealed at 1350°C for 6 hr, following the O^+ implantation at the energy of 180 keV, with the dose of 4 x 10^{17} cm^{-2}. The projection range for the implanted ions toward the SiGe layer is estimated as 0.4-0.45 μm. After this SIMOX process, the flat buried oxide layer is formed among the SiGe layer.

Fig. 2 shows the RBS spectrum from both samples. The three layers; the SiGe layer over the buried oxide, the buried oxide layer, the SiGe layer under the oxide, are clearly distinguished. Table 1 summarizes the Ge content of each layer estimated from RBS. The Ge content under the buried oxide is significantly small comparing to the Ge content of SiGe on the buried oxide, because of the Ge diffusion toward the substrate during the annealing. As shown in fig. 3, the Ge content of SiGe on the buried oxide in the sample A keeps 10 %, which does not decrease after the annealing. This fact means that the buried oxide layer acts as the blocking wall for the Ge diffusion. However, in the sample B, the Ge content of SiGe on the buried oxide decreases after the annealing indicating that the Ge atoms pass through the buried SiOx layer and diffuse during the early stage of the annealing, where the complete buried oxide has not been formed yet. These results suggest that the Ge diffusion during the SIMOX annealing must be considered into account to design the thickness of SiGe layer before SIMOX process.

3. Proposal of SiGe double layer buffer on buried oxide

Although the higher Ge content of SiGe layer is necessary to introduce higher strain in Si grown on the SiGe layer and higher mobility in the strained films, It has already been reported that the formation of the buried oxide among the SiGe layer with high Ge content is difficult because of the limitation of the annealing temperature [3]. In order to solve this problem, we propose the SiGe double layer structure which has a SiGe layer with higher Ge content grown on the SiGe layer with lower Ge content (fig. 4). It is expected that the SiGe layer with lower Ge content, directly bonded to buried oxide, acts as the dislocation absorber and, as a result, the strain of the second SiGe layer is relaxed. The $Si_{1-x}Ge_x$ (X=0.075) layer (the first layer) on the buried oxide is formed by the SIOX technique as the substrate. Next, the $Si_{1-x}Ge_X$ (X=0.18) layer of 0.2 μm thick (the second layer) and a Si layer of 20 nm are re-grown on the substrate. Fig. 5 shows the depth profiling of Ge and O measured by sputtering Auger electron spectroscopy. It is confirmed that the designed two step Ge profile is obtained. Fig. 6 shows the cross-sectional TEM image of the sample. The existence of dislocations at the regrowth interface indicates the partial relaxation of the second layer, suggesting that the first SiGe layer is suitable for the buffer layer which absorb the dislocation.

The strain in each layer of the double layer structure and that in the $Si_{1-x}Ge_X$ (X=0.18) layer of 0.2 μm thick which directly grown on a Si substrate were measured by RAMAN spectroscopy (fig 7). In the double layer structure(fig. 7a), the observed two peaks correspond to the first and the second layers. The peak shift corresponded to the second layer indicates that the layer is 55 % relaxed. This value confirms that the second layer (X=0.18) is partially relaxed on the first layer (X=0.075), even though the $Si_{1-x}Ge_X$ (X=0.18) layer directly grown on the substrate is fully strained (fig. 7b). This result means that the SiGe double layer structure provides the higher strain in Si layer than that obtained by the conventional structure.

4. Conclusion

Two ideas which bring the highly strained Si layer on insulator were presented and verified. These technique enables to fabricate the high performance MOSFET device with the strained Si layer.

Reference

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[2]T.Mizuno, et.al. IEDM Technical digest, p.934 (1999)
[3]Y.Ishikawa, et.al., Appl.Phys.Lett. Vol.75, p.983 (1999)

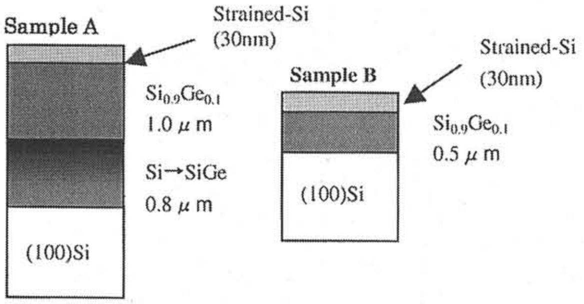

Fig. 1 Schematic illustration for two samples to evaluate the Ge diffusion.

	On Oxide	Under Oxide
Sample A	10%	3.0%
Sample B	3.5%	1.1%

Table.1 Comparison of Ge content in each layer measured by RBS.

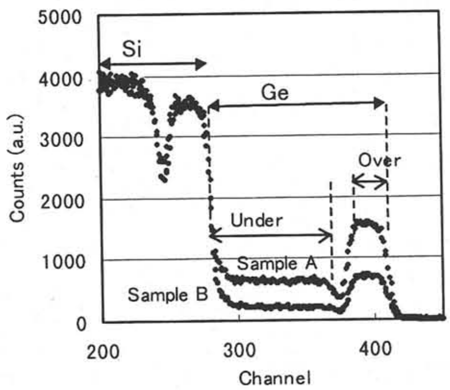

Fig. 2 RBS spectrum from each sample.

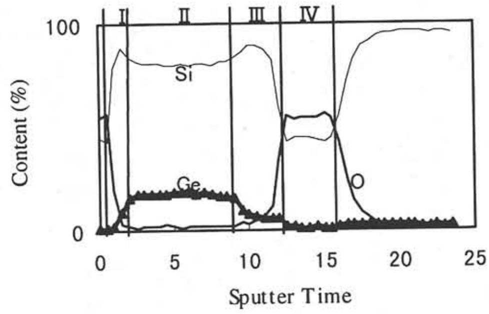

Fig.5 Depth profiling of Ge and O in the SiGe double layer structure measured by AES.

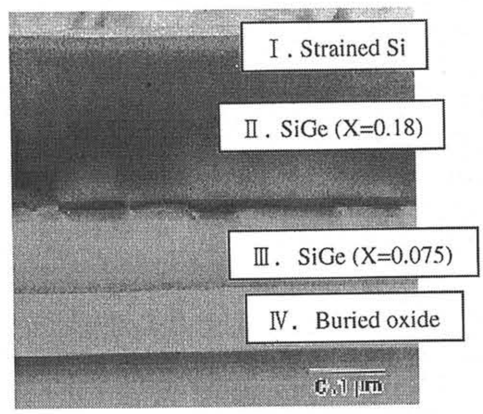

Fig.6 Cross-sectional TEM image of the double layer structure.

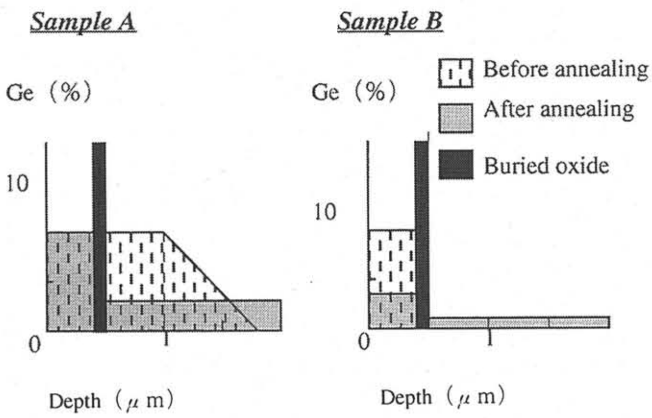

Fig. 3 Schematic illustration for Ge diffusion during annealing.

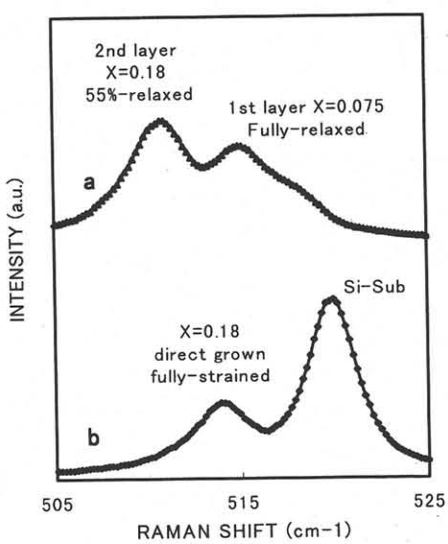

Fig.7 RAMAN spectrum from the SiGe double layer structure (a) and the conventional structure (b).

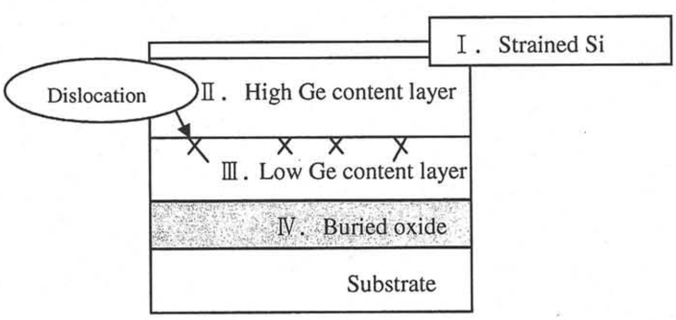

Fig. 4 Schematic illustration of SiGe double layer structure.