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C-8-3

Optimization of Selective Epitaxy Process for Elevated Source/Drain Applicable to 0.15 μm Fully Depleted CMOS on 25 nm SOI

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1. Introduction

Fully-depleted (FD) SOI-MOSFETs are attractive for future low-power devices because of their near-ideal subthreshold behavior and low parasitic source/drain (S/D) capacitance. In order to realize a 0.1-μm generation FD SOI-MOSFET, suppression of the short-channel effects (SCE) is most important. It is known that the suppression of SCE on FD SOI-MOSFET is achieved by thinning of the SOI film for the channel. However, thinning of SOI films was accompanied by an increase in the parasitic S/D resistance. By optimizing the salicidation conditions for $CoSi_2$ [1] or $TiSi_2$ [2], it is reported that the series resistance of S/D can be improved down to a 30 nm SOI film thickness (t_{SOI}). However, in the case of t_{SOI} less than 30 nm, it becomes more difficult to reduce the S/D resistance because the amount of Si is insufficient for making di-silicide. For reducing the S/D resistance, a selective Si epitaxy technique in the S/D region [3] and Co salicidation were performed. However, we found that patterned SOI films of less than 30 nm thickness agglomerate during the epitaxy process. In this paper, we report on the optimization of the selective epitaxy process and fabrication of 0.15 μm FD SOI-CMOS on 25 nm SOI.

2. Device Fabrication and Epitaxy Method

A schematic cross section of typical process steps is shown in Fig. 1. The ELTRAN wafer with a buried oxide layer thickness of 100 nm was used. After the formation of a conventional LOCOS isolation, a gate- oxide layer of 3.5 nm thickness was grown. After poly-Si and SiN deposition, electron-beam lithography was used to pattern the gate electrode. After LDD implantation, the first side-wall was formed by the deposition and reactive etching of 30-nm-thick SiO_2 in order to separate the gate and elevated S/D. Then a 40-nm-thick nondoped selective epitaxial Si growth (SEG) film was deposited on the S/D region. After the second side-wall formation and removal of the SiN on the gate, S/D implantation was performed. After RTA at 1000℃ for 10 seconds, Co salicidation (Co = 8 nm) was performed.

The SEG process is as follows. After RCA cleaning with HF dip, the wafers were loaded into a load-lock chamber. They were subsequently loaded into a CVD reactor and H_2 bake, and a SEG film was deposited by LP-CVD using SiH_2Cl_2, HCl and H_2 gases, continuously.

3. Selective Epitaxy for Elevated Source/Drain

A SEM photograph of the active pattern after SEG at 800℃ with H_2 baking at 930℃ is shown in Fig. 2(a). In this experiment, t_{SOI} is approximately 30 nm. It is found that the SOI and SEG film were agglomerated during the epitaxy process. In order to suppress the agglomeration, the H_2 baking temperature was reduced to 880℃. As shown in Fig. 2(b), the amount of agglomeration was improved. At 830℃, agglomeration did not occur, but the surface of the film was rough, as shown in Fig. 2(c). At 800℃, SEG film deposition was impossible.

The SIMS profile of the film in Fig. 2(b) is shown in Fig. 3. Carbon contamination and an oxide, which could not be removed during the H_2 baking, remained at the surface of the SOI film. Figure 4 shows the cross-sectional TEM photograph of the Si surface after the first side-wall etching. An amorphous layer is observed to a depth of 3 nm from the Si surface. It is supported that this layer is contaminated by C and prevents SEG film growth. By removing this C-contaminated Si amorphous layer with plasma pretreatment in CF_4 and O_2, the SEG film was stably grown even at 800℃ H_2 baking, as shown in Fig. 5.

The relationship between the length of agglomeration (L_{agg}) and t_{SOI} was investigated at various annealing temperatures in H_2. The L_{agg} was defined as how far does SOI film shrink from the boundary between the SOI film and the LOCOS region. As shown in Fig. 6, there was a critical thickness for stable epitaxial growth at each annealing temperature. It appears that it was necessary to reduce the temperature to about 680℃ for the SEG process of 0.15 μm FD SOI-CMOS on 25 nm SOI.

4. Device Characteristics

A cross-sectional TEM photograph of a fabricated 0.15 μm FD SOI-MOSFET before Co salicidation is shown in Fig. 7. The SEG film of 40 nm thickness on the S/D region was formed on the SOI layer of channel thickness 25 nm.

The I-V characteristics for 0.15 μm N- and P-MOS devices are shown in Figs. 8 and 9. The NMOS shows good subthreshold characteristics and on-current. On the other hand, the PMOS shows a slightly higher subthreshold factor and a small drain current compared with those of NMOS. This is because the gate and S/D for PMOS became offset structures due to the fact that the diffusion length of the dopant for LDD is less than that expected.

The dependence of S/D resistance (R_{SD}) on t_{SOI} is shown in Fig. 10. The SEG film thickness was 40 nm and Co-silicide was formed. The sheet resistances for N- and P-active on 25 nm SOI (channel thickness of MOSFET) are very low, 5Ω/□ and 7.5 Ω/□, respectively.

5. Conclusion

We have investigated the selective epitaxial Si growth on a very thin SOI layer for the fabrication of 0.15 μm gate length FD SOI-CMOS. It was shown that the SEG film agglomerated under the high-temperature Si-epitaxy process. However, by optimizing the epitaxy process, it was found

that a 0.15-μm-gate-length FD SOI-CMOS device exhibiting good performance could be fabricated by using an elevated S/D and Co salicidation. This device shows a good short-channel-effect immunity and a low S/D resistance.

Acknowledgment

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References

[1] K. Imai et al., Symp. VLSI Tech., T12-3, 1998.
[2] C. Raynaud et al., IEEE Int. SOI Conference Proceedings, pp. 86-87, 1999.
[3] M. Cao et al., IEEE Electron Device Let, vol. 18, No. 6, pp. 251-253, 1997.

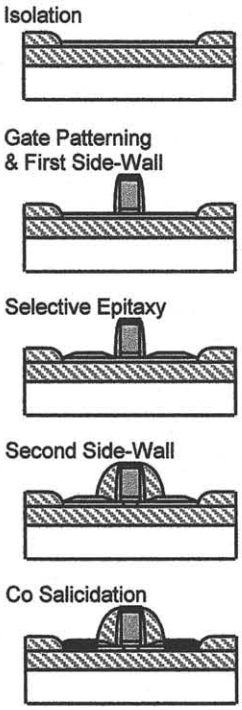
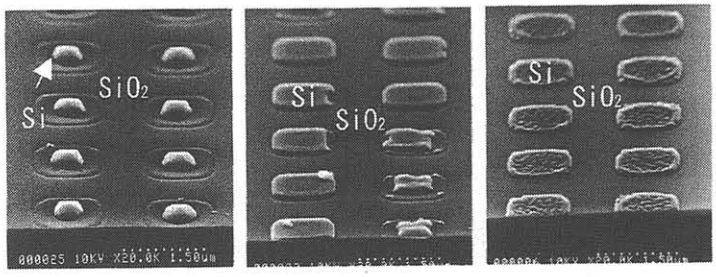


Fig. 1. Schematic cross section of typical process steps.



(a) (b) (c)

Fig. 2. SEM photograph of active pattern after SEG at 800℃ with H_2 baking (a) at 930℃, (b) at 880℃ and (c) at 830℃.

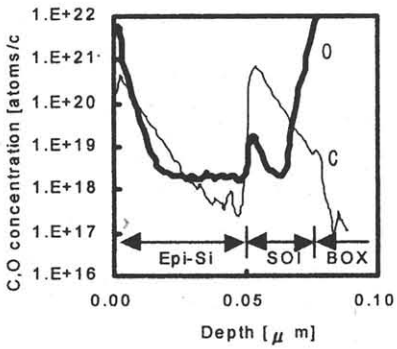


Fig. 3. SIMS profile of SEG film for the conditions of Fig. 2(b).

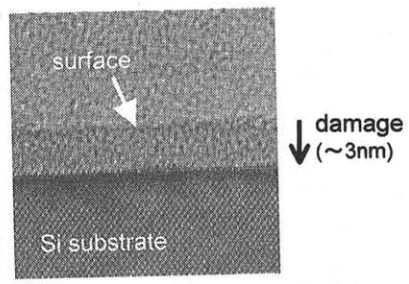


Fig. 4. Cross-sectional TEM photograph of the surface damage caused by C contamination.

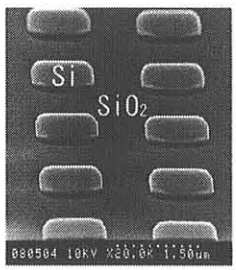


Fig. 5. SEM photograph of active pattern after SEG at H_2 baking at 800℃ with removing C contamination.

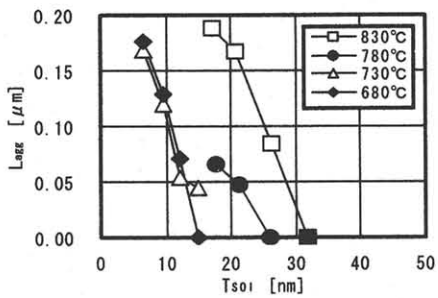


Fig. 6. Dependence of agglomeration length (L_{agg}) on SOI film thickness.

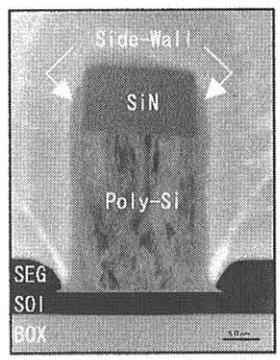


Fig. 7. Cross sectional TEM photograph of a fabricated 0.15 μm FD SOI-MOSFET before Co salicidation.

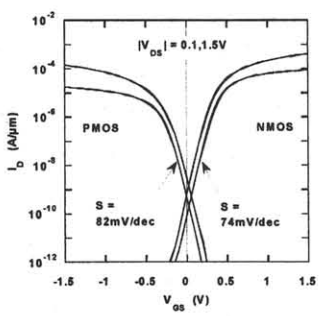


Fig. 8. Subthreshold characteristics of 0.15 μm FD SOI N- and P-MOS.

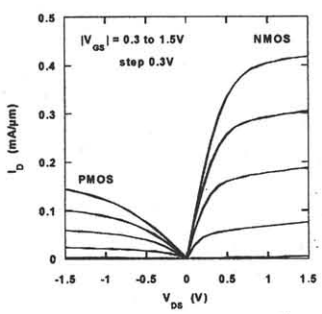


Fig. 9. I_d-V_{ds} characteristics of 0.15 μm FD SOI N- and P-MOS.

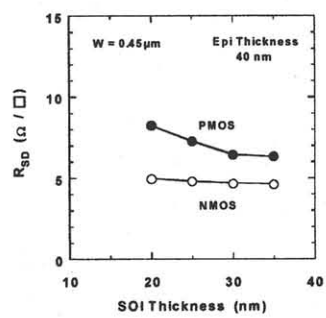


Fig. 10. Dependence of S/D resistance (R_{SD}) on t_{SOI}