Extended Abstracts of the 2000 International Conference on Solid State Devices and Materials, Sendai, 2000, pp. 478-479

C-8-4

Advanced Co Salicide Technology for Sub-0.20 μm FD-SOI Devices

Takashi Ichimori, Norio Hirashita and Jun Kanamori

Oki Electric Industry Co. Ltd., VLSI Research Center
550 Higashi-asakawa, Hachioji, Tokyo, 193-8550, Japan
Phone: +81-426-62-6112, Fax: +81-426-67-8367, e-mail: ichimori683@oki.co.jp

1. Introduction

Fully-depleted SOI devices have excellent characteristics for low power applications, such as low subthreshold swing, low source/drain (S/D) capacitance and small floating body effect compared to bulk devices or partially-depleted SOI devices[1,2]. These features derive from the thin SOI film whose typical thickness is less than 50nm, however, this makes device fabrication extremely difficult.

The major problem is current leakage between the SOI and the substrate through the buried oxide layer (BOX leakage). It is supposed that the BOX leakage is generated via a formation of threading pinholes through the BOX layer at the contact opening. Thus, to suppress these pinholes, thickness uniformity of the SOI or, more straightforward, uniformity of silicided SOI is essential. Another issue to be cleared is reduction of the parasitic source/drain series resistance. To achieve reasonably low series resistance, it is reported that the silicide thickness should be less than 80% of whole the SOI thickness when the contact resistivity between silicide and Si is greater than $1\times10^{-7}\Omega\text{-cm}^2$ [3].

From these requirements a highly stable and controlled formation of ultra-thin silicide (less than 40nm-thick) under a limited Si film thickness must be established.

This work presents an impact of salicide process on ultra-thin (20-50nm) SOI ULSI device fabrication by comparing the advanced Co salicide with conventional Ti salicide and Co salicide. The new salicide was applied to sub-0.20μm FD CMOS devices fabricated on ultra-thin SOI substrates and the device operation was confirmed.

2. Experimental

Commercially available SIMOX wafers were used as the starting material. The SOI films were first thinned by a conventional oxidation and oxide strip, where the final Si thickness, tSi, ranged from 20 to 50nm. After a LOCOS isolation and channel doping were conducted, gate oxide (4.5nm) and gate polysilicon were formed. The gate was patterned by Lg=0.15-10μm, then followed by spacer formation, S/D implantation, and various salicide processes using Ti or Co were applied. Each salicide process was carried out in 2step annealing with employing TiN capping in the 1st RTA. The surface roughness of silicides was evaluated by SEM/AFM and the silicide defects and detailed morphology were investigated using FIB/XTEM method. Electric properties were discussed in relation with these silicide properties.

3. Results and discussion

Fig.1 is a cross-sectional TEM image of defects in a SOI film silicided by Ti. Titanium silicide is prone to agglomerate at C49 to C54 phase transformation, which results in worsening of sheet resistance. BOX leakage current was measured for each salicide process on $S=1mm^2$ SOI island with 400k contacts. The yield for Ti salicide was a little over 10% (Fig.2).

Compared to Ti salicide, conventional Co salicide made slight improvement in the BOX leakage property as shown in Fig.2. AFM scanning on the silicide surface after the 2nd RTA revealed that the typical peak-to-valley height was 20-30nm in 10μm square area. However, defects in silicided SOI were still present as shown in Fig.3, where the pinhole was formed when the contact etching was performed onto a thin spot of silicided SOI. Since these thin spots possibly coincide with triple junctions of the silicide grains and/or local thinning of SIMOX[4], the BOX leakage strongly depends on the grain size of the silicide and the roughness of the SOI wafer.

Our advanced Co salicide process drastically improved the surface morphology of silicided SOI. In the AFM measurement of silicide surface after the 1st RTA and the 2nd RTA, typical peak-to-valley heights were reduced to approximately 4nm and 10nm respectively. The obtained sheet resistance was 7Ω/sq. both on the S/D and the gate electrode which were silicided with 6nm-thick Co. Line width dependence was checked from 10μm to 0.1μm, but no degradation was detected. In this new salicide the key process step is that the 2nd RTA for silicidation is applied after the NSG interlayer formation and the contact opening. The NSG layer works effectively to suppress surface roughening of silicide and accordingly eliminates deep slits

formation at grain boundaries. Fig.4 is a cross-section of pMOSFET produced by the advanced Co salicide. Highly flat and uniform silicided SOI was obtained by the NSG capping at the 2nd RTA. The excellent BOX leakage characteristic shown in Fig.2 resulted from contact opening onto the flat silicide surface, which is only available right after the 1st RTA.

Using the new Co salicide, the BOX leakage yield was evaluated for various SOI film thickness on an SOI island of 400μm square area with 160k 0.2μm ϕ contacts (Fig.5). The result demonstrates that the 25nm-thick SOI is tolerable for device production with present SIMOX substrates, which falls in sub-0.15μm regime. However, even by the use of the advanced Co salicide, the Box leakage still strongly depends on the SOI thickness. The present SIMOX wafer contains high density of deep local thinning in the order of 10nm, which currently determines the lower limit of the SOI thickness for ULSI application.

MOSFET operation was confirmed in Lg=0.15μm n and pMOSFET fabricated on 22nm-thick SOI. In Fig.6, the subthreshold swings were 68 and 76mV/dec respectively, and floating body effect was negligible. Another feature of these MOSFETs is that the S/D Si was completely consumed by silicide, but the series resistance of nMOSFETwas kept under 500Ω-μm, which is comparable to those where less than 80% of the S/D SOI is silicided. Such low resistance is indicative of a surprisingly low contact resistivity between $CoSi_x$ and Si.

4. Conclusions

An advanced Co salicide and a novel MOSFET structure were developed for sub-0.20μm FD SOI device. With the new salicide, the BOX leakage was completely eliminated down to tSi=25nm using commercial SIMOX wafers. The key technology for 0.15μm FD SOI device production was established.

References

[1] K. Imai et al., Symp. VLSI Tech., p116 (1998).

[2] J. Chen et al., Symp. VLSI Tech., p25 (1999).

[3] L. T. Su et al., IEEE EDL15, 363 (1994).

[4] W. Maszara, 98 IEEE Int'l SOI Conf. Short Course.

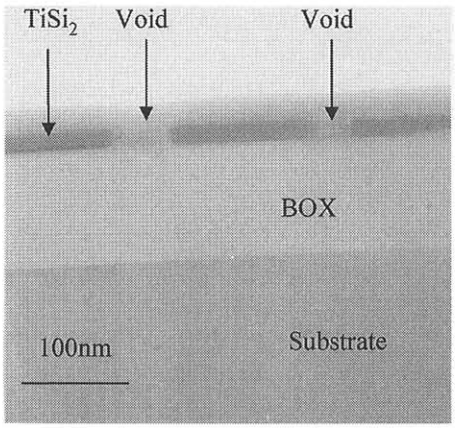

Fig. 1 XTEM photograph of agglomeration in Ti-salicided SOI

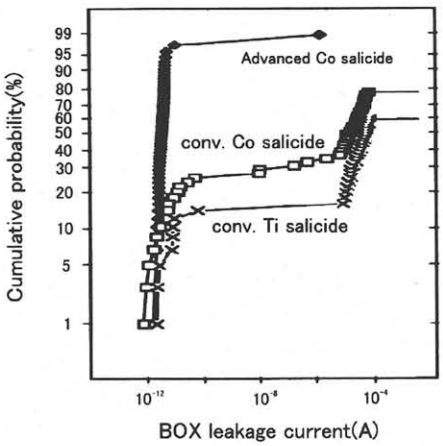

Fig. 2 Distribution of the BOX leakage current for various salicide process (T_{Si}=46nm)

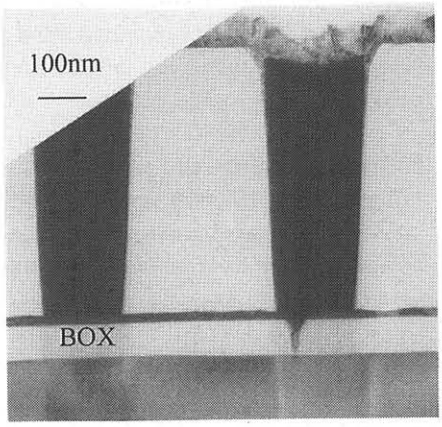

Fig. 3 XTEM photograph of the BOX leakage point for conventional $CoSi_2$ S/D layer (T_{Si}=46nm)

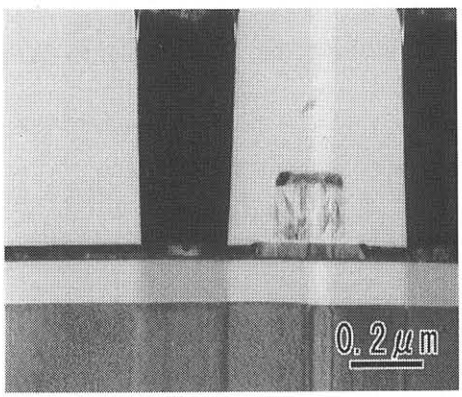

Fig. 4 XTEM picture of a pMOSFET produced by the advanced Co salicide (T_{Si}=46nm)

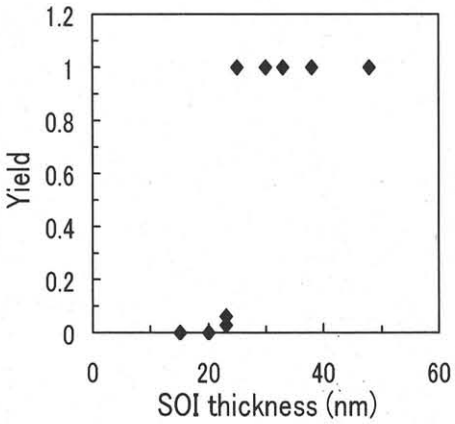

Fig. 5 BOX leakage yield on 400μm sq. SOI island with 160k 0.2μm contacts for various SOI thickness

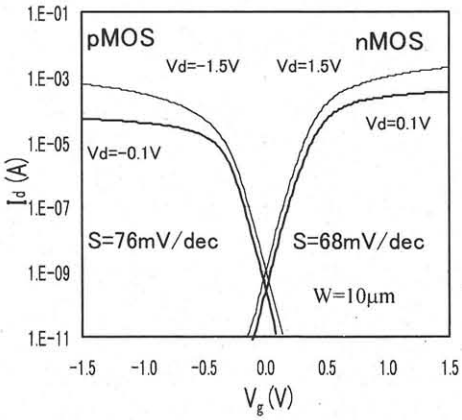

Fig. 6 Subthreshold characteristics of L_g=0.15μm n and pMOSFET on 22nm-thick SOI