Extended Abstracts of the 2000 International Conference on Solid State Devices and Materials, Sendai, 2000, pp. 480-481

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Proposal of a Partial-Ground-Plane(PGP) Silicon-on-Insulator(SOI) MOSFET for Deep Sub-100-nm Channel Regime

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1. Introduction

The main problem in miniaturizing MOSFETs is the short-channel-effect (SCE) [1]. It is well known that ground-plane (GP) or double-gate (DG) SOI MOSFETs offers reduced SCE [2]. Unfortunately, most GP-SOI MOSFETs have a very large subthreshold slope (S) [2], and the threshold voltage (V_{th}) of n^+-poly-Si DG-SOI nMOSFETs is usually very low [3], while V_{th} of p^+-poly-Si DG-SOI nMOSFETs is comparatively very high [4]. DG-SOI MOSFETs also have many weaknesses from the viewpoint of the process technology. Consequently, issues remain in achieving practical short-channel SOI MOSFETs.

This paper proposes a new device structure that overcomes the above-mentioned shortcomings. Simulations are used to confirm the DC and switching performances of the proposed device. A comprehensive discussion of performance is provided.

2. Device structure and simulations

The proposed device structure, shown in Fig. 1, is called the "partial-ground-plane (PGP)" SOI MOSFETs. This device structure has two-isolated ground plane regions below the buried oxide layer which are p-type regions with doping levels of the order of 10^{20} cm^{-3}. They are placed under the source and drain regions in order to control the electric field around the junction regions. Parameter L_1 is the space between the PGP region and the source or drain junction edge. The width of the PGP region (L_2) and the depth of the PGP region are both sets to 10 nm. The gate oxide thickness (t_{ox}), the Si layer thickness (t_s) and the buried oxide thickness (t_{box}) of single-gate (SG), GP, DG and PGP SOI devices are 3 nm, 5 nm and 10 nm, respectively.

3. Simulation results and discussion

V_{th} dependence on channel length (L) is shown in Fig. 2 for the SG, GP, DG and PGP SOI nMOSFETs. Drain voltage (V_d) is 1.0(V). For the PGP SOI device, V_{th} characteristics are shown in Fig. 2 for three values of L_1. Since the device has a n^+-poly-Si gate, the DG SOI device offers normally-on operation. On the other hand, the GP SOI device has a preferable threshold value from the viewpoint of device design, while the SG SOI device has a slightly low V_{th}. The V_{th} characteristics of PGP SOI devices depend on parameter L_1. Setting L_1 to 20 nm seems better from the viewpoint of SCE suppression.

The dependence of S on L is shown in Fig. 3 for the same devices shown in Fig. 2. The DG SOI device shows the best S performance as expected [3,5]. The GP SOI device shows the worst S performance. Though the PGP SOI device has a larger S value than the SG and DG SOI devices, its S value is about 70 mV/dec. for the PGP SOI device with L_1 of 20 nm.

It is considered that a large part of the source- and drain-induced electric fields at the channel region are terminated at the PGP region. This suppresses the drain-induced barrier lowering (DIBL) effect at the SOI layer/buried oxide layer interface.

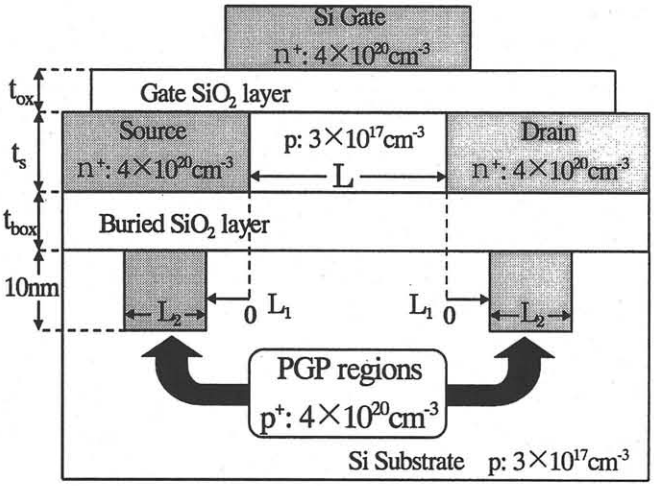

Fig. 1. Schematic cross section of the partial-ground-plane (PGP) SOI MOSFETs device (W=1 μm).

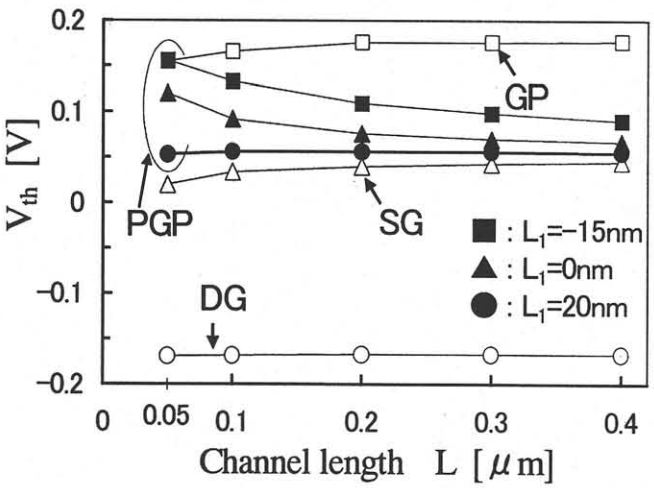

Fig. 2. V_{th} dependencies on channel length for SG, GP, DG and PGP SOI MOSFETs (V_d=1V). V_{th} is the gate voltage providing $I_d=10^{-7}$ A for W/L=1.

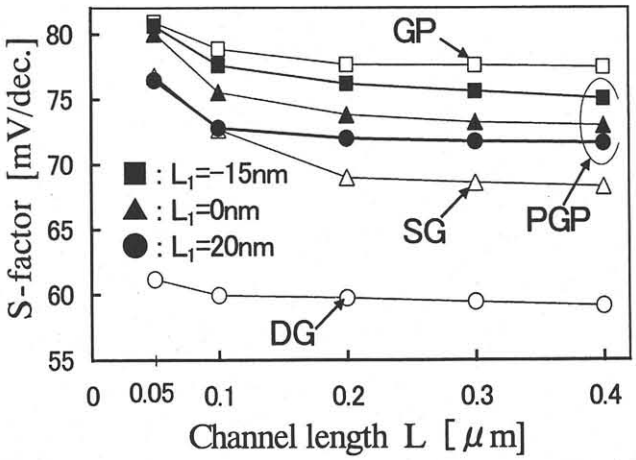

Fig. 3. S-factor dependencies on channel length for SG, GP, DG and PGP SOI MOSFETs (V_d=1V).

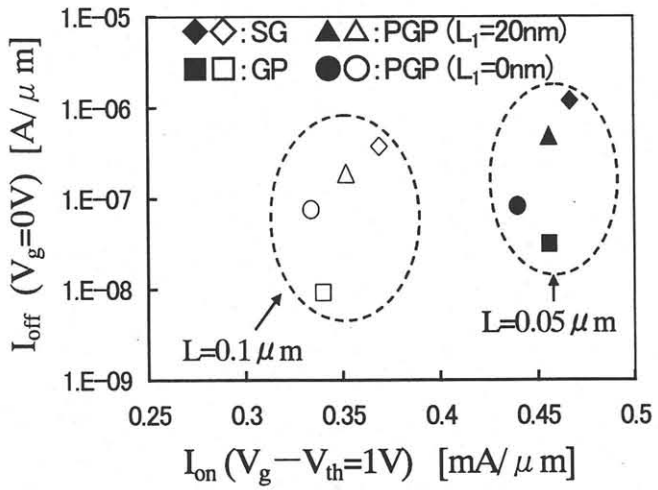

Fig. 4. I_{on}-I_{off} characteristics of SG, GP and PGP SOI MOSFETs (V_d=1V).

Next, the on/off current characteristics at V_d =1 V are summarized in Fig. 4 for 0.1 and 0.05 μm channel devices; the gate voltage of (V_{th} + 1V) is applied to compare device driveability. Fig. 4 shows that the SG device has the best driveability and the worst leakage current because of its poor SCE; the driveability of the PGP device, which has lower SCE, is comparable to that of the SG device when L_1 is designed appropriately. The GP device apparently has a lower leakage current than the PGP device because the GP device has a higher threshold voltage. Fig. 4 also shows that the PGP device with a smaller L_1 has a lower leakage current.

Switching performances at V_d = 1V are compared for the SG, GP and PGP devices with a 0.05 μm channel. Dynamic simulation results are shown in Fig. 5, where a resistance load is used. The SG device shows the fastest response, while the time-zero V_d value ("high level") is degraded because of the SCE. On the other hand, the PGP

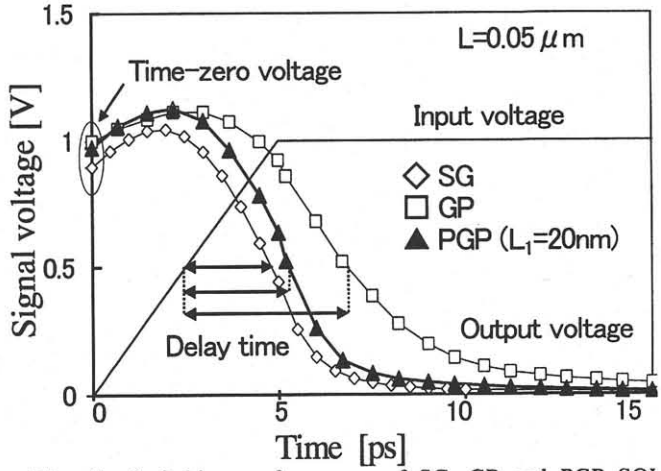

Fig. 5. Switching performances of SG, GP and PGP SOI MOSFETs at V_d of 1V.

devices clearly exhibit superior performance compared to the GP device because of the lower parasitic capacitance under the source and drain regions. Therefore, the PGP device has promising performance for deep-sub-0.1 μm SOI MOSFETs because it has an appropriate threshold voltage with low SCE, lower leakage current and a high switching speed.

4. Conclusion

This paper has proposed the partial-ground-plane (PGP) SOI MOSFETs. The PGP device minimizes the short-channel-effect compared to the conventional SG device because the gate-induced field in the SOI layer is held high by the partial-ground-plane region. This results in a lower stand-by leakage current. The PGP device shows much better switching performance because of its smaller parasitic capacitance comparing compared to the conventional ground-plane device. Thus, the PGP SOI MOSFETs is a promising candidate for future deep-sub-0.1 μm LSIs.

References

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