# Reduced Reverse Narrow Channel Effect in Thin SOI nMOSFET's

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### Abstract

The effects of narrow channel width on the threshold voltage of deep submicron silicon-on-insulator (SOI) nMOSFET's with LOCOS isolation have been investigated. The reverse narrow channel effect (RNCE) in SOI devices is found to be dependent on the thickness of the active silicon film. A thinner silicon film is found to depict less threshold voltage fall-off. These results can be explained by a reduced oxide/silicon interface area in the transistor width direction, thus the boron segregation due to silicon interstitials with high recombination rate is reduced.

## Introduction

Reduced body effects, freedom from latch-up, and excellent soft-error immunity have made SOI technologies very attractive for future high-speed operation CMOSFET's. SOI MOSFET's also offer significant power reduction as compared with bulk MOSFET's due to the reduced parasitic capacitance [1]. Meanwhile, the demand for low-power applications has called for the use of transistors with narrowchannel width [2]. It is therefore technologically important to study the characteristics of narrow-channel SOI MOSFET's suitable for low-power and high-speed digital and analog circuit applications. More recently, reverse short channel effect (RSCE) in SOI MOSFET's has also been reported to depend on the silicon film thickness (Tsi) [4-5]. However, to the best of our knowledge, the dependence of the reverse narrow channel effect (RNCE) on the Tsi has never been reported. In the present paper we report, for the first time, the effects of silicon film thickness on the RNCE. A model is also proposed to explain the observed phenomenon.

## **Device Fabrication**

N<sup>+</sup> poly-Si gate n-channel MOSFET's were fabricated on SIMOX wafers with Tsi ranging from 40-190 nm and a 400 nm buried oxide. LOCOS was performed to fully consume the active silicon layer in the isolation region. Channel implant was performed by BF<sub>2</sub> (50 keV, 6×10<sup>12</sup> cm<sup>-2</sup>), followed by the growth of a 4 nm gate oxide at 800°C with in-situ HF-vapor cleaning. Afterwards, a 200-nm poly-Si layer was deposited, patterned, and etched to form the transistor gates. A shallow N<sup>+</sup> S/D extension implant with As (5 keV,  $1 \times 10^{15}$  cm<sup>-2</sup>) was then performed, followed by the formation TEOS spacer. Then, an As implant at 10 keV with a dose of  $5 \times 10^{15}$  cm<sup>-2</sup> was performed to form the n<sup>+</sup>-doped source/drain regions. Wafers received a RTA at 1000°C for 10 sec and were then processed through a standard backend flow through metallization. Finally, wafers were sintered at 400°C for 30min in forming gas.

#### **Results and Discussion**

Figure 1 shows the measured n-channel threshold voltage Vth at Vsub = 0V as a function of channel width for the T-gate test structure as shown in the Fig. 2 with different active silicon film thickness. Here  $\Delta$ Vth is defined as Vth (W) – Vth (W=20µm). The threshold voltage is measured at Vd =

50 mV at the intercept point on the Vg axis of the Id versus Vg curve extrapolated from the point of maximum slope. Although devices with thick silicon film depict serious reverse narrow channel effect (i.e., drastic Vth fall-off with decreasing channel width), the threshold voltage fall-off is alleviated as the silicon thickness is decreased.



Figure 1. Threshold voltage roll-off as a function of the channel width for samples with various silicon film thicknesses.



Figure 2. The test gate structure of T- and H- gate. H-gate devices are edgeless and the T-gate devices have a LOCOS-isolation edge in the width direction.

Figure 2 shows the test structure. It should be noted that the H-gate devices are edgeless (i.e., the active channel region does not interface with LOCOS isolation edge). In contrast, the T-gate devices have a LOCOS-isolation edge in the width direction as shown in the plot. Figure 3 shows the body effect factor ( $\gamma$ ) ratio {Gamma (W=0.6  $\mu$ m)/Gamma (W=20  $\mu$ m)} versus the silicon film thickness for both T-and H-gate test structures as shown in the Fig. 2. In the case of H-gate devices,  $\gamma$  ratio is almost independent of Tsi,

depicting a value close to one. This is believed to be primarily due to their edgeless feature, so that they are immune to any effects due to boron segregation into the isolation oxide in the width direction [6]. Therefore,  $\gamma$  ratio is almost close to one irrespective of Tsi. On the other hand, Tgate devices not only depict lower  $\gamma$  ratio than H-gate devices but also show an apparent dependence on Tsi. Obviously, the difference in the behavior between T-gate and H-gate devices must be due to the existence of edge oxide. However, the dependence of  $\gamma$  ratio for T-gate on Tsi is somewhat unexpected.

To explain this intriguing phenomenon, a physical model is proposed as shown in Figure 4. Since it is well known that silicon interstitials generated by source/drain implantation tend to move toward the Si/SiO<sub>2</sub> interface and recombine there during subsequent thermal processing [7]. When Si interstitials are moving toward the Si/SiO2 interface, channel impurities such as boron will diffuse and segregate into oxide simultaneously. This is the so-called transient enhanced diffusion (TED) that causes RSCE and RNCE [7-8]. Figure 4 shows a schema of the 2-D flux of excess interstitials caused by implantation damage or arsenic deactivation. The recombination of the diffusion-enhancing interstitials at the Si/SiO<sub>2</sub> interface in the width edge gives rise to the observed Vth fall-off dependence in the width direction and the reduction of RNCE in thinner Tsi SOI devices as show in Figure 1. A thinner Tsi and its corresponding smaller cross-sectional silicon/oxide interface area in the width edge results in a smaller number of interstitials arriving and recombining there. Thus, a larger ratio of channel boron atoms diffuse and segregate into the buried oxide instead of the isolation oxide in the width edge, thus leading to the reduction of RNCE in SOI devices with thinner Tsi. Figure 5 shows the relationship between RSCE and RNCE for different Tsi devices. It is clearly shown that the reduced RSCE in thin Tsi devices is accompanied with reduced RNCE. This is consistent with previous report that the reduced RSCE in thinner SOI devices is primary due to the decrease of the lateral distribution of Si interstitials resulted from their high recombination velocity at the buried oxide [5]. Vth shift due to RSCE is in fact in proportion to the Vth shift due to RNCE as shown in Fig. 4. This result supports our proposed model that Si interstitials with higher recombination velocity at the buried oxide will reduce the lateral redistribution in both length and width directions.

### Conclusion

We have investigated the effects of silicon film thickness on the reverse narrow channel effect of SOI nMOSFET's. Devices with thinner Tsi show a reduced reverse narrow channel effect as well as reverse short channel effect. Furthermore, Vth shift due to RSCE is found to be proportional to the Vth shift due to RNCE as Tsi increases. The experimental findings can be explained by a decrease of cross-sectional silicon/oxide interface area in the width edge so that the boron segregation into oxide due to silicon interstitials is reduced, leading to a reduced RNCE in SOI nMOSFET's with thinner silicon film.

#### References

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Figure 4. Schematic of the mechanism of RNCE for thin and thick SOI MOSFET's.



Figure 5. Relationship between RSCE and RNCE for different silicon film thickness.