

C-9-1

A Single Chip Automotive Control LSI Using SOI BiCDMOS

Kazunori Kawamoto, Shoji Mizuno, Hirofumi Abe, Yasushi Higuchi,
Seiji Fujino and Isao Shirakawa¹

Electronics Device R&D, DENSO CORPORATION

5 Maruyama, Ashinoya, Kouta, Nukata, Aichi 444-0193, Japan

Phone:+81-564-56-7480 Fax:+81-564-56-7913 e-mail:kazunori_kawamoto@mgt.net.denso.co.jp

¹Department of Information System Engineering, Graduate School of Engineering,
Osaka University

1. Introduction

The number of electronic control systems in a car is increasing to cope with growing demands for safety and ecology. For example, safety operation of automobile air bag systems has been improved. In some systems, crush gravity sensors and air bag systems are installed in narrow space of handles and side doors. In this case, the ECU's (Electronic Control Units) should be as small as possible by eliminating electronic parts inside. The authors propose that thick film SOI BiCDMOS with trench dielectric isolation is a suitable device technology for integrating the parts, such as a 32 bit RISC micro controller, an accurate non-crystal oscillator and an ESD immune LDMOS (Lateral DMOS), into a single chip. This IC monitors signal wave forms from gravity sensors, distinguishes a heavy crush, and fires an air bag at a proper timing, without any miss-operation.

2. Pattern layout and device structure

Fig.1 shows a pattern layout of a single chip for an air bag. The size is $10.5 \times 11.24 \text{ mm}^2$, the number of mask steps of the process is 33, the pin count is 118, and the design rule is $0.8 \mu\text{m}$.

A 32bit Reduced Instruction Set Computer (RISC) is selected as a Center Processing Unit (CPU) for this single chip, for its high performance and core compactness is considered to be most suitable. It has a set of 118 instructions, specified for automobiles, and One Time Programmable ROM (OTP)[1].

LDMOS in Fig.2 is capable of driving 1.5 amperes for triggering an air bag. Its structure has p- and n-well on a n-type SOI active layer, which improves ESD (Electrostatic Discharge) immunity[2]. The CPU also includes a clock generator of DPLL (Digital Phase Lock Loop), which is accurate and temperature compensated by trimming metal thin-film resistance in the chip, and eliminates an external crystal (Fig.3)[3].

3. Wafer process

Starting SOI wafers have an active n⁺ on n⁺ silicon layer of $15 \mu\text{m}$ thickness, on a buried thermal silicon dioxide layer of $1.5 \mu\text{m}$ thickness. Then the active layer is dry-etched vertically to dig trenches of $2 \mu\text{m}$ width according to the

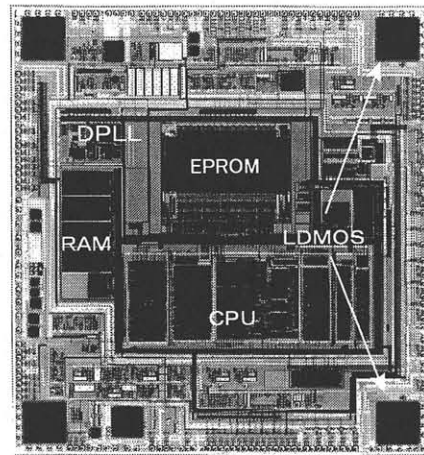


Fig.1 Single chip IC to control an air bag.

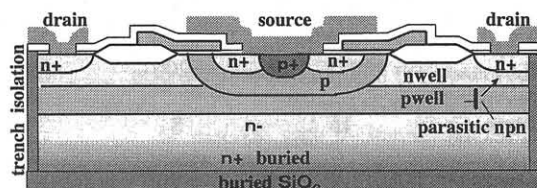


Fig.2 Cross section view of LDMOS.

isolation pattern. The trenches are thermally oxidized and filled back with CVD poly silicon to form dielectric isolation. Then the wafers are flattened by Chemical Mechanical Polishing (CMP).

Logic CMOS is $0.8 \mu\text{m}$ rule, and has double poly-silicon layers for EPROM (Electrically Programmable ROM) and double Al layers for inter connection.

Between the Al layers, thin and high resistivity, 15 nm thick and $500 \Omega/\square$, CrSi metal layer is deposited by sputtering. This resistance has extremely low temperature coefficient of $\pm 10 \text{ ppm}/^\circ\text{C}$, and it can be calibrated initially to a desired value by laser trimming at wafer probing process.

The laser beam of near infra red wave length is focused to the CrSi layer through CVD SiO_2 and silicon nitride passivation layer, and the beam trims off the resistance until DPLL reaches the expected time accuracy.

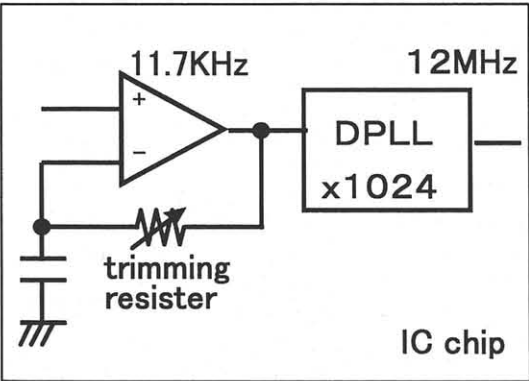


Fig.3 DPLL with a trimming resistor.

4. Results and discussion

As instruction execution speed of the RISC CPU is 4 times as fast as the conventional 16bit CISC, its clock speed can be as low as 6MHz, instead of 16MHz for an air bag control, which eliminates dissipation current and noise emission. An OTP ROM proves enough retention life time of more than 100years at 150°C. Table 1 summarizes the architecture and performance, comparing RISC and CISC.

Table 1 Comparison of this 32 bit compact RISC and a conventional 16bit CISC used for an air bag systems.

	32 bit RISC	16 bit CISC
core size[mm ²] (0.8um)	2	8
performance[MIPS] (Dhrystone)	12	3
instructions	118	>200
general registers	16	8
code size[Kbytes] (air bag)	20	20

As for LDMOS, ESD robustness is 1.2KV, about 2.5 times of the conventional junction isolation LDMOS. And for DPLL, 3 sigma deviation of the time accuracy of clock is 0.1% at room temperature, and 1% in the temperature range of -40~120°C(Fig.4).

4. Conclusions

A single chip automotive control IC has been described, which integrates different kinds of devices, has developed by using SOI BiCDMOS, and has confirmed the expected high performance by setting an example of an air bag control LSI.

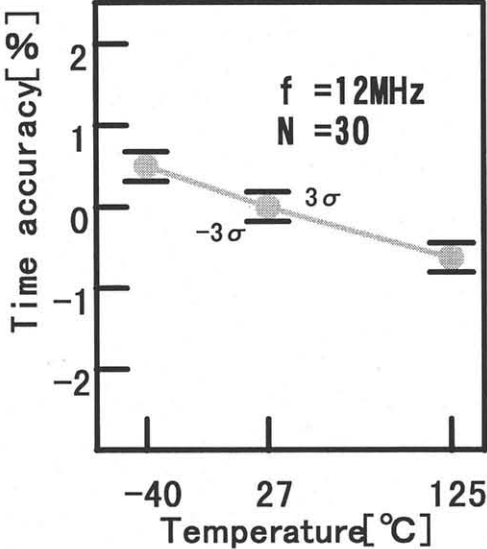


Fig.4 Temperature dependence of the oscillator.

Acknowledgments

The authors would like to express sincere appreciation to all the contributors to this work for their cooperation.

References

- [1] Hiroshi Hayakawa, et. al., "Small size and high-speed CPU for automobile control," IEICE Gen. Con. 1999,p. 407, in Japanese.
- [2]T. Efland, et. al., "An optimized RESURF LDMOS power device module compatible with advanced logic processes," IEEE IEDM Tech. Digest, pp. 237-240, 1992.
- [3]Takamoto Watanabe, et. al., "A CMOS Time-to-Digital Converter LSI with Half- Nanosecond Resolution Using a Ring Gate Delay Line," IEICE TRANS ELECTRON.,VOL. E76-C, NO. 12 DECEMBER 1993, pp.1774-1779