Extended Abstracts of the 2000 International Conference on Solid State Devices and Materials, Sendai, 2000, pp. 490-491

C-9-3 (Invited)

Substrate Characteristics of Nanocleave SOI Wafers

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Abstract

A room temperature, atomic-layer cleaving process for fabrication of thin-SOI wafers is described. The SOI wafer properties include an as-cleaved surface finish in the range of 1-3 Å and Si layer thickness range of under 3%.

I. Introduction

A key to the expansion of the use of SOI-based devices is the development of efficient production technologies for fabrication of high-quality, controlled-cost SOI wafers. An important goal is the elimination of the use of chemical-mechanical polishing or similar methods for Si device layer smoothing and damage removal. These steps add a significant cost burden on the process and compromise the efforts to achieve precise control on the Si layer thickness and crystal quality. This goal has been achieved in a novel process for fabrication of SOI wafers by layer transfer techniques which results in an as-cleaved Si surface finish with an RMS roughness of ~2 Å. The Si film thickness uniformity is routinely better than 2% for 100 to 200 nm layers on 200 mm wafers. Because the bonding and cleaving steps in the layer transfer process are done at room temperature, the process is easily controlled and well suited for high-volume fabrication.

II. The Nanocleave™ Process

The Nanocleave™ Process uses four main steps: (Fig. 1).

1. A "donor" layer of silicon is formed on a silicon wafer. This silicon layer is free of crystal defects (octahedral voids, oxygen precipitates, carbon sites, etc.). Next, a high-quality thermal oxide layer is grown on the donor wafer.
2. A layer with modified mechanical strength, or "cleave plane," is formed beneath the "donor" wafer surface.
3. A "handle" wafer is then bonded to the donor wafer using a plasma treatment of the bond surfaces. This process forms a bonded interface that is up to 30 times stronger than a conventional wet bonding process [1].
4. The donor and handle wafers are separated at room temperature by an atomic layer cleaving process. The wafer can be annealed (to increase the SOI bond strength) or smoothed in an epi-reactor process [2] (to provide sub-Angstrom surface finish).

III. Si Roughness, and SOI Edge Definition

The Si-SOI layer thickness is determined by the as-formed device layer thickness before bonding and cleaving. The surface finish after final anneal is in the range of 1 to 2 Å and does not vary strongly with the area of surface sampled (Figs. 2, 3). Surface roughness is <1 Å for wafers finished with an epi-smoothing step [2]. The atomic-layer selectivity of the location of the cleave plane across the wafer surface also provides a clean and well formed SOI layer edge profile following cleaving. The Si layer edges are formed along the diagonal (111) and (110) planes. The final edge taper of the BOX portion of the SOI edge depends on the bond strength anneal and final clean processes (Fig. 4). These crystallographic edge tapers are significantly more regular than those achieved by thermal separation methods.

IV. Hg-MOSFET characteristics

Pseudo-MOSFET [3] measurements with a 4-Dimensions "horseshoe-dot" Hg-probe yield good transistor characteristics (Fig. 5). Gate bias testing gives sub-threshold slopes of 65 mV/decade for thin-SOI layers on 100 nm BOX.

V. Summary

A room-temperature cleaving process has been developed which achieves atomic-layer cleaving and provides a direct method for fabrication of thin-SOI wafers and other forms of laminated electronics with high materials quality.

References

1. S.N. Farrens et al., J. Electrochemical Soc. 142(11) (1995) 3949-3955.
2. A. Thilderkvist et al., to be presented at IEEE SOI 2000, Wakefield, MA.
3. S. Cristoloveanu, S.S. Li, "Electrical Characterization of SOI Materials and Devices", Kluwer Academic (1995).

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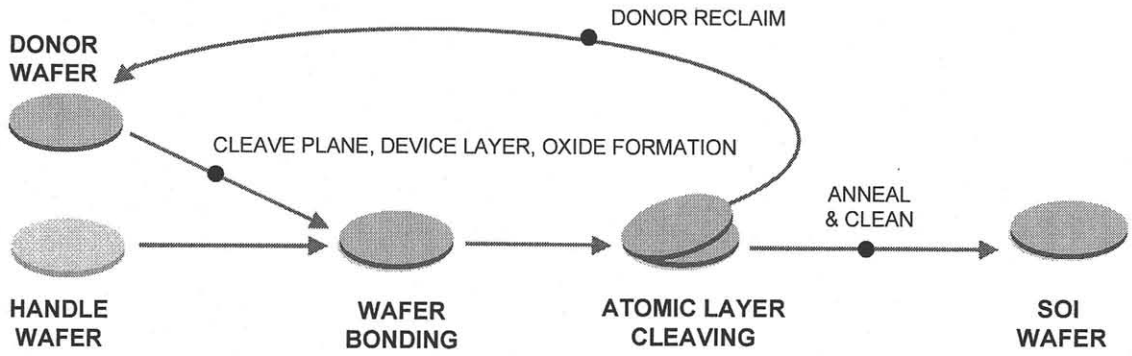
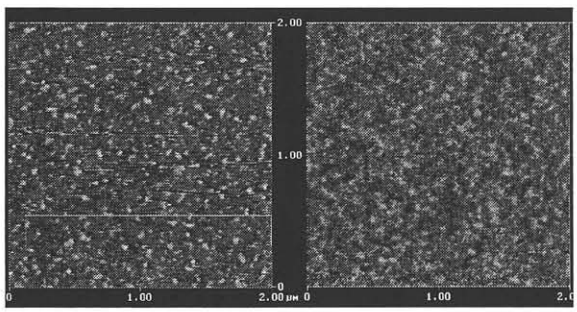


Figure 1. Nanocleave™ process flow.



After Cleave & Clean: 2.3 Å RMS

After Anneal & Clean: 1.3 Å RMS

Figure 2. AFM images of as-cleaved and final product SOI wafers (2x2 um scan).

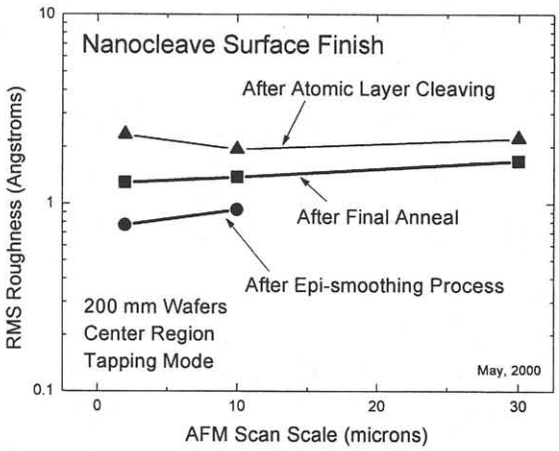


Figure 3. AFM measurements of Si roughness after cleaving, after final anneal and after an epi-

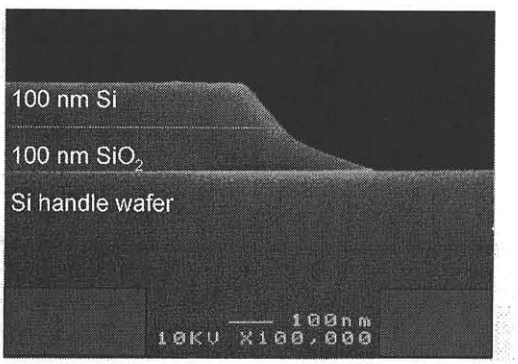


Figure 4. SEM cross-section view of the SOI edge taper for a 100 nm Si(110) layer on a 100 nm BOX.

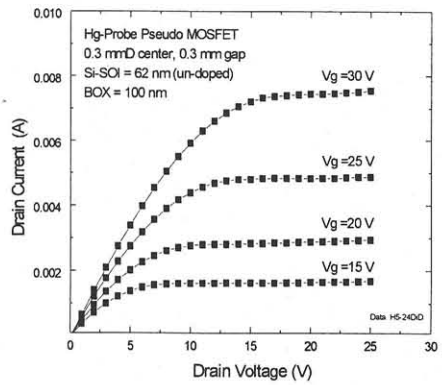


Figure 5. Hg–probe pseudo-MOSFET characteristics of an SOI wafer with Si-SOI thickness of 62 nm and a BOX of 100 nm.