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Single-Electron Transistors with Two Self-Aligned Gates

Katsuhiko Nishiguchi and Shunri Oda

Research Center for Quantum Effect Electronics, Tokyo Institute of Technology,
2-12-1 O-okayama, Meguro-ku, Tokyo 152-8552, Japan
Phone: +81-3-5734-2542 Fax: +81-3-5734-2542 e-mail: knishi@pe.titech.ac.jp

1. Introduction

As one of future devices with low power consumption, single-electron transistors (SETs) attract much attention because they work with a smaller amount of electrons than ordinary devices. However, SETs are very sensitive to the background charge accumulated on a system. So we fabricate an SET with two self-aligned gates in order to control the background charge. These gates are fabricated near a Coulomb island by EB evaporation using aluminum at the same time. In aluminum systems, quantum effects are minor compared to semiconductor systems, so the observed characteristic does not include other effects except for Coulomb blockade effect. This allows us to measure ideal characteristic. Moreover, the etching characteristics of SOI/SiO_2 system to make a shadow mask for Al evaporation enables SET dots of 50nm to be fabricated by high throughput sub-micron fabrication system (120nm).

2. Fabrication

We use a silicon-on-insulator (SOI) substrate with a thickness of 100nm. A resistivity is 0.001Ωcm. By electron beam (EB) lithography using ZEP-520 resist diluted with ZEP-S (1:3), a 120nm-wide channel is patterned as shown in Fig. 1(a). SOI is etched till a thickness 30nm by electron-cyclotron-resonance reactive-ion-etching (ECR -RIE) using CF_4 (Fig. 1(b)). After removing the resist, the sample is oxidized. The oxide thickness is 90nm. This means that a thinner area of SOI, which is etched before, is completely oxidized. And the shape of un-oxidized SOI becomes trapezium as Fig. 1(c). Then, for planerization of the surface, we use an etch-back process. The sample is coated with a 200nm-thickness ZEP-520, followed by ECR-RIE. Then, a 50 nm-thick SiO_2 layer is deposited with the plasma enhanced chemical vapor deposition using tetraethoxysilane (TEOS). For the fabrication of two gates and a Coulomb island, we pattern as Fig. 1(d) by EB lithography. The width of a narrow line is 120nm. Then TEOS SiO_2 is etched by ECR-RIE till SOI layer appears. A characteristic of ECR-RIE makes a shape of etched SiO_2 tapered as Fig. 1(e). Thus the size at a bottom of etched SiO_2 becomes smaller (50nm) than the size patterned by EB lithography (120nm). Then SOI appearing on the surface is selectively etched by isotropic plasma etching using CF_4+5% O_2 gas mixture. This process causes an under-etching of Si. Finally, aluminum film with a thickness of 20nm is deposited by EB evaporation, followed by a lift-off. At this time, a Coulomb island is formed on an area of etched Si because TEOS SiO_2 serves as a shadow mask. Fig. 1(f) shows a Coulomb island with a length of 50nm and a height of 20nm.

2. Results and Discussion

Fig. 2 (a) shows the current characteristic as a function of voltage between electrode A and B, shown in Fig. 1(d), at 10K. Gates are grounded. The current is suppressed at a low bias voltage. Fig. 2(b) indicates that a current oscillates periodically as a gate voltage V_{g1} increases. These characteristics prove that Coulomb blockade effects are observed. From these curves, we estimate values of two tunnel junctions' parameters as Fig. 2(d). Moreover, all peaks are roughly the same shape. In ordinary silicon SETs, it is often reported that the shape and the height of peaks fluctuate because of an energy quantization or a change of a potential profile of SOI channel. The fluctuation results in a fluctuation of devices and a difficulty of an operation when SETs are used in logics. However, this device is composed of metal Coulomb islands and a gate does not cover a SOI channel, so it is estimated that a fluctuation of peaks is small. Moreover, by applying an electric field by the other gate electrode V_{g2} to Coulmb island, a Coulomb oscillation is shifted as shown in Fig. 2(c). This indicates that we can adjust the background charge of each SET, which improves the problem of a background charge when SETs are used in logic devices.

3. Conclusion

We can observe Coulomb blockade effects in a device composed of a silicon channel and aluminum island and gates. By taking advantage of asymmetric etching characteristics, the Coulomb island is smaller than the lithography pattern. Actually, we can decrease the size of the island to 50nm with 0.12μm fabrication trend, which is expected to be the next benchmark for high throughput optical lithography.

Acknowledgments

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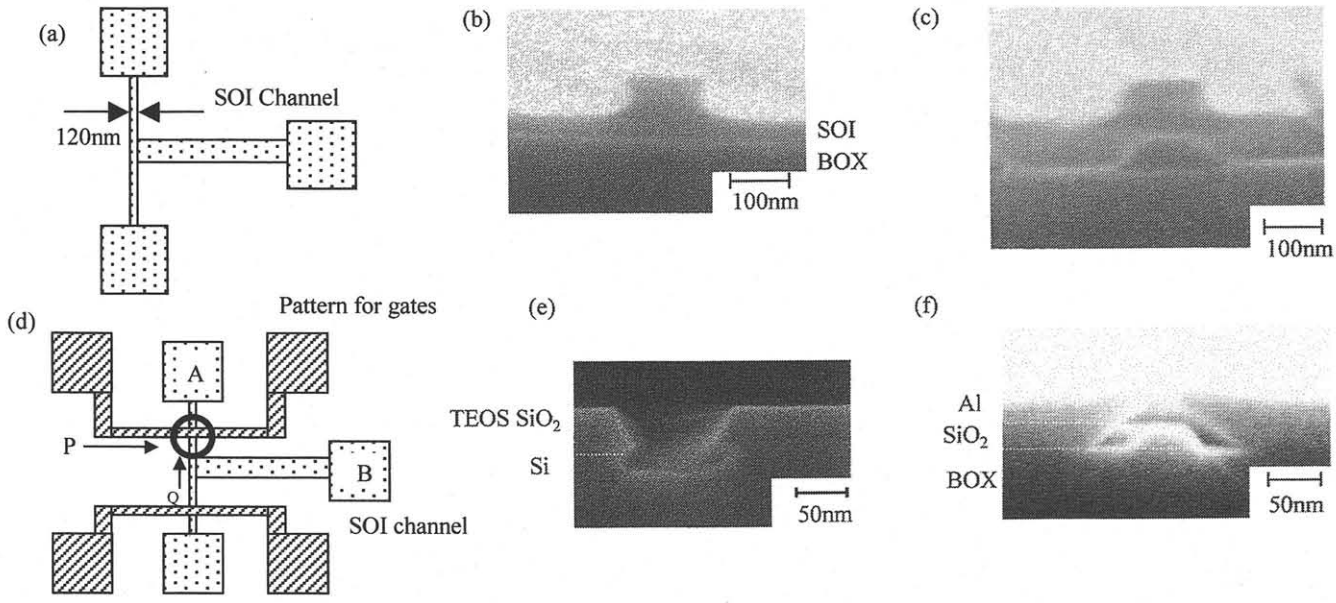

Fig. 1 Device fabrication process. (a) Channel pattern of SOI (b) Cross sectional SEM image of etched SOI (c) Cross sectional SEM image of the oxidized channel (d) Pattern of gates and island (e) Cross sectional SEM image of etched SiO_2 by ECR-RIE and etched SOI by plasma etcher in a circled area of (d) in the direction of arrow P(f) Cross sectional SEM image after metal evaporation in the circled area from the direction of arrow Q.

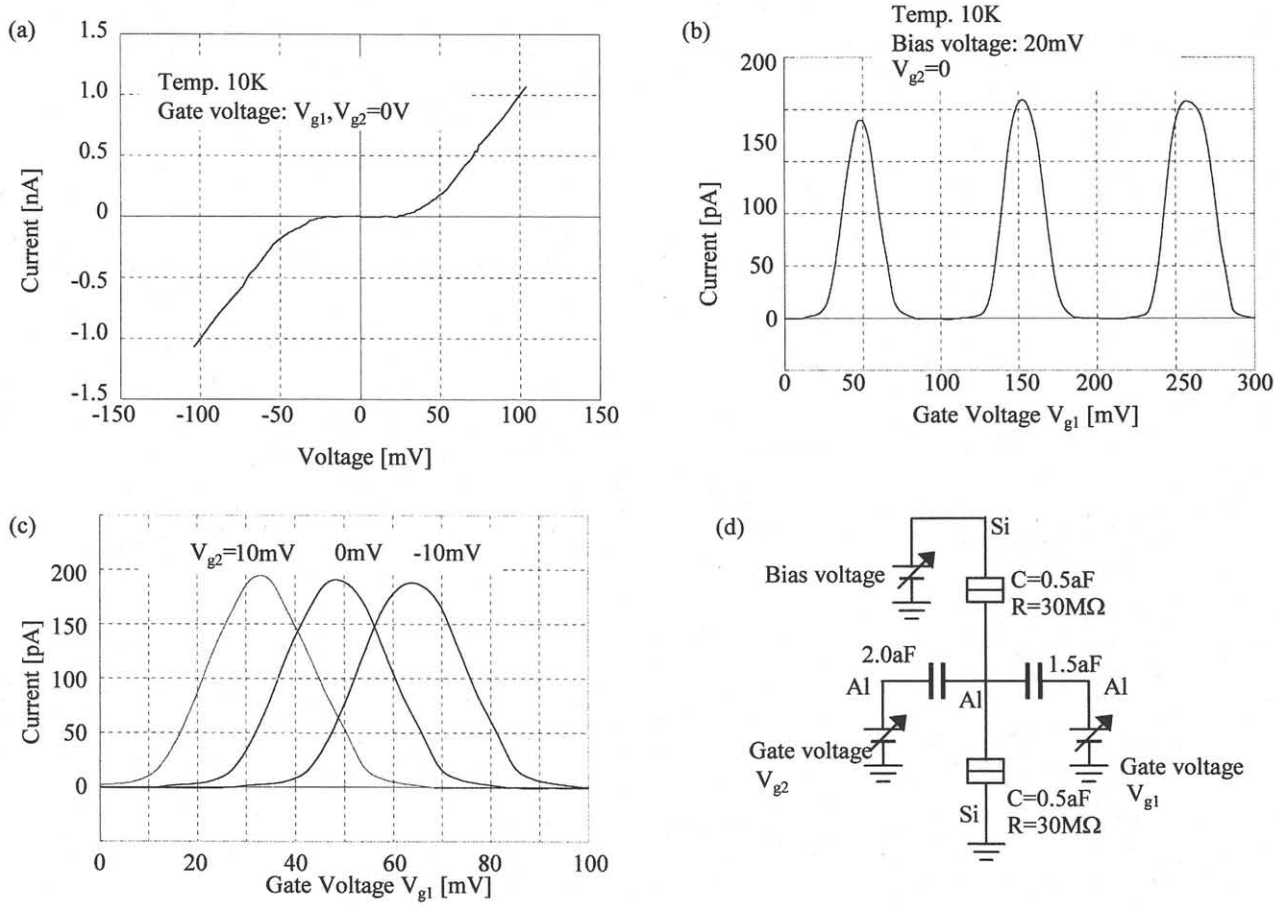

Fig. 2 (a) Current characteristic as a function of bias voltage. Gate electrode are grounded. (b) Current characteristic as a function of gate voltage V_{g1}. Bias voltage is 20mV, and at V_{g2}=0, (c) at various V_{g2}. All measurements are at 10K. (d) An equivalent circuit.