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Structural and Electrical Characterization of Nanocrystalline Silicon (nc-Si) Single Electron Transistors

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1. Introduction

In the future in microelectronics technology, both the lateral and vertical dimensions of the devices will be reduced from the sub-micron scale to the nanoscale. Devices will be smaller in lateral size and in depth. Silicon based materials have the potential to be tailored chemically to meet these requirements.

Nanocrystalline silicon (nc-Si) is one such silicon based material that contains silicon grains with size that can be controlled to 5 nm[1], embedded in an amorphous silicon (a-Si:H) matrix. Due to the small grain size there is a potential application for this material in fabricating single electron transistors (SETs).

2. Material and device fabrication

A 50 nm thick nc-Si film was grown on a 150 nm thick buried oxide layer with a crystalline silicon substrate. A VHF plasma-enhanced chemical vapor deposition (PECVD) method from a SiF_4, H_2 and SiH_4 gas mixture[2] was used.

The SET was fabricated by defining the device structure with polymethyl methacrylate (PMMA) resist using electron beam lithography. After development the nc-Si film was etched in a 1:1 plasma of $SiCl_4$ and CF_4 (see Fig. 1).

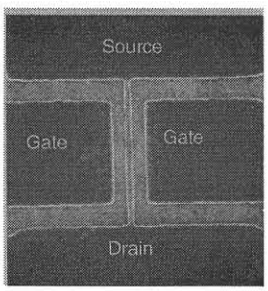

Figure 1 A scanning electron micrograph of a fabricated device. There are two side gates separated from the channel by 120 nm.

3. Experimentation

In order to characterize electrically the dependence of electron transport in the nc-Si material on the physical dimensions of the conducting channel, we have fabricated 1 μm long channels with width of 40, 50 and 60 nm.

In addition, we have investigated the effects of defect state density on the electrical characteristics of the devices by modifying the defect state density and grain size using annealing at 1000°C in oxygen or argon.

Structural characterization of the film was performed by transmission electron microscopy (TEM), Raman spectroscopy, reflection high energy electron diffraction (RHEED), spectral ellipsometer (SE) and atomic force microscopy (AFM).

4. Structural Characterisation

From Raman spectroscopy and SE we found the crystal fraction of nc-Si to be ~60%. This high crystal fraction is attained by the use of fluorinated source gas and careful selection of gas flow rate ratio as reported in ref. 2. The RHEED pattern showed that the crystal fraction and grain size increases as film thickness increases from 10 nm to 50 nm and that it includes (111) preferentially oriented grains. From TEM analysis, we found the mean grain size to be 5 nm. We also found a uniform grain distribution using AFM.

After argon annealing of the nc-Si the TEM micrograph showed a columnar structure of grains 50 nm in height and ~17 nm in lateral diameter.

The Raman spectra show no decrease in the c-Si peak intensity after oxidation. However, there was a reduction in the a-Si:H peak intensity suggesting that most of a-Si:H matrix was oxidized to form a-SiO_x.

In films of cross-sectional area 0.5 mm wide x 10 to 1000 nm thick films, the Hall mobility increases as film thickness increases from 10 nm to 50 nm and exhibits saturation for thicker films. This indicates that the crystal fraction of 60% is high enough for crystalline grain percolation and the conduction path is via the crystalline grains. It is expected that crystalline grains are isolated from each other as channel width decreases to a dimension comparable to grain size.

5. Electrical results

Measurements of the oxidized SET were taken over a temperature range of 17 K to 300 K. Current conduction was

negligible at 17 K but at 19 K we observed regularly spaced steps in the current-voltage characteristic with a period of ~200 mV. No conduction was observed for the narrower channel SETs.

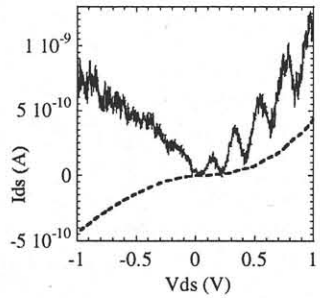

Fig. 2 Current–voltage plot of oxidized SET (dotted line) at 4.2 K, channel width of 60 nm. dI/dV (solid line) depicting step-like structures.

We have also observed regular gate conductance oscillations at 19 K as shown in Fig. 3. The period of oscillation is ~200 mV.

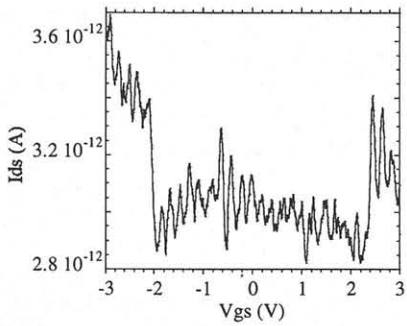

Fig. 3 Gate conductance oscillations with Vds=48 mV.

To explain our results we note that the Mott equation[3] for variable range hopping (VRH) conduction in *d*-dimensions is:

$$\sigma = \sigma_0 \exp(-(T_0/T)^{1/(d+1)}) \quad (1)$$

Plotting $\ln(\sigma)$ against $T^{-1/3}$ we were able to obtain a good linear fit thus, demonstrating two-dimensional VRH conduction in the oxidized SET.

For the argon annealed SET we also observed single electron charging effects (see Fig. 4). The Coulomb gaps for 40, 50 and 60 nm channel width are 10 mV, 5.5 mV and 2 mV respectively.

There are multiple smaller peaks superimposed on a larger peak (see Fig. 5). The periods of the smaller and larger peak oscillations were estimated to be 4.2 mV and 500 mV respectively.

5. Conclusions

Coulomb blockade effects were observed in oxidized and annealed SETs fabricated on nc-Si films prepared by PECVD at 300°C.

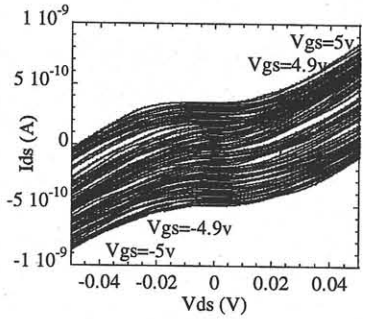

Fig. 4 Current-voltage characteristics of annealed SET with gate sweep from –5 V to 5 V. Measurement performed at 4.2 K.

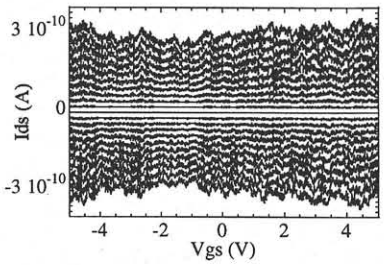

Fig. 5 Gate conductance oscillations of annealed SET with Vds = -20 mV to 20 mV in steps of 2 mV.

In annealed nc-Si SETs, TEM analysis shows that the grains are columnar in shape 50 nm in height and ~17 nm in lateral diameter. The island capacitance as obtained from our measurements gives an island size of ~22 nm. Hence, the island size corresponds well to the grain size.

In the oxidized SETs two-dimensional variable range hopping conduction was observed. As our nc-Si film is highly doped the Fermi level is located close to the bottom of the conduction band of c-Si which suggests that the hopping sites are impurity dopant atoms.

The resistance of the oxidized SET was found to be higher than the annealed SET. This could be attributed to the formation of thick SiO_X at the grain boundaries which we associate with the tunnel barrier.

Acknowledgements

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References

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