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Novel Si Quantum Memory Structure with Self-Aligned Stacked Nanocrystalline Dots

Ryuji Ohba, Naoharu Sugiyama, Junji Koga, Ken Uchida and Akira Toriumi
Advanced LSI Technology Laboratory, TOSHIBA Corporation, 8, Shinsugita-cho, Isogo-ku, Yokohama 235-8522, Japan
Phone/Fax: +81-45-770-3687/+81-45-770-3578, E-mail: oba@amc.toshiba.co.jp

I. INTRODUCTION

In the Si nanocrystal floating gate MOS memory [1], the tunneling oxide between the Si dots and the channel is very thin. Hence, it is very important to find a technology to improve the charge retention.

In this work, we fabricate a Si self-aligned double dot memory shown in Fig.1, in which the floating gates are double-stacked Si dots. In this memory, the Coulomb blockade can affect the charge retention effectively, since a high charging energy in the lower Si dot suppresses the charge leak between the upper dot and the channel. We show that the retention characteristics of the self-aligned double dot memory is better than the usual single-layer Si dot memory. This indicates a new approach to obtain a Si dot memory with a long retention time.

II. EXPERIMENTAL

Fig.2 shows the fabrication process of the self-aligned double dot memory. A tunnel oxide (3nm thick) was thermally grown on Si substrate. A 5nm thick a-Si layer was formed on the tunnel oxide by CVD [2], and a 3nm thick oxide was thermally grown on the surface of the a-Si layer (Fig.2(a)). The Si crystalline dots were formed by LPCVD on the a-Si layer (Fig.2(b)). The Si self-aligned double dot structures can be obtained by oxidizing the a-Si layer completely, because a-Si can remain only immediately below the Si dots by adjusting the oxidation time (Fig.2(c)). We oxidized the a-Si layer in dry O_2 at 700 °C, and observed that the oxidization rate is faster for the a-Si than for the crystalline dot. The top oxide (20nm thick) by LPCVD was formed between the gate and the double dot structures, so the total top oxide thickness between the gate and the upper dots was about 30nm. Fig.3 shows a cross-sectional TEM view of the double-dot memory. We can make sure that a lower Si dot exists immediately below an upper Si dot.

We also fabricated the usual single-layer Si dot memory in which the a-Si layer deposition and the following oxidation processes were omitted. Hence, the tunnel oxide thickness, Si dot size and the top oxide thickness were 3nm, 15nm and 20nm, respectively.

III. RESULTS AND DISCUSSION

Fig.4 show the $I_D - V_G$ characteristics in the usual single-layer dot memory. We found the V_{TH} shift between the forward and backward sweeps. No V_{TH} shift was found in the reference MOSFET with no Si dot. The V_{TH} shift between the forward and backward sweeps was also found in the self-aligned double dot memory as shown in Fig.5. In the double dot memory, the memory effect is due to the charging to the Si double dot structures, since no V_{TH} shift was found in the corresponding reference MOSFET of which gate oxide thickness is 33nm (3nm from the tunnel oxide, 10nm from the completely oxidized a-Si and 20nm from the LPCVD top oxide).

Next, we compare the retention characteristics between the double dot memory and the usual single-layer dot memory. In order to investigate the effects of the double dot structure on the charge retention accurately, we compare the retention characteristics of these memories in the inversion region, since the surface potential flexibility and the carrier number shortage also affect the charge retention remarkably in the depletion region [3].

Fig.6 shows the retention characteristics of the usual dot memory after writing/erasing at $V_G - V_{TH} = 8/-5$ V. The retention time for the single-layer Si dot structure is short in the inversion region [3]. In Fig.6, we find that the memory window disappears at 100 sec. On the contrary, in the retention characteristics of the self-aligned double dot memory shown in Fig.7, the memory window is still finite at 1000 sec. This shows that the charge retention is improved by using the double dot structures. Therefore, there is the possibility that the formation of the self-aligned stacked dot structure in the Si dot memory is a promising technology to improve the charge retention.

IV. CONCLUSION

We fabricated the novel Si dot memory structure with self-aligned stacked nanocrystalline dots, and found that the charge retention of the double dot memory is better than that of the usual Si dot memory. This shows the possibility that the Si self-aligned double dot memory is a strong candidate to develop the Si quantum dot memory technology.

Acknowledgment

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[2] N.Sugiyama et al.,: J.Crystal Growth **192** (1998) 395.
[3] R.Ohba et al.,: Ext. Abs. of SSDM (1999) p86; Jpn. J. Appl. Phys. **39** (2000) 989.

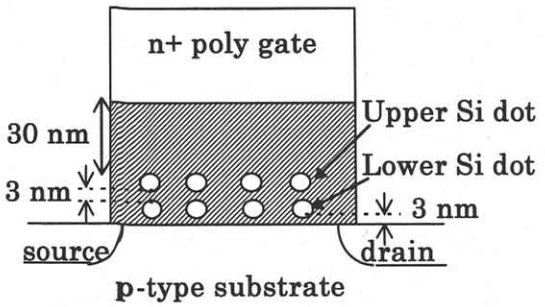

Fig.1 A schematic diagram of Si self-aligned double dot memory. The floating gates are self-aligned double stacked Si dots.

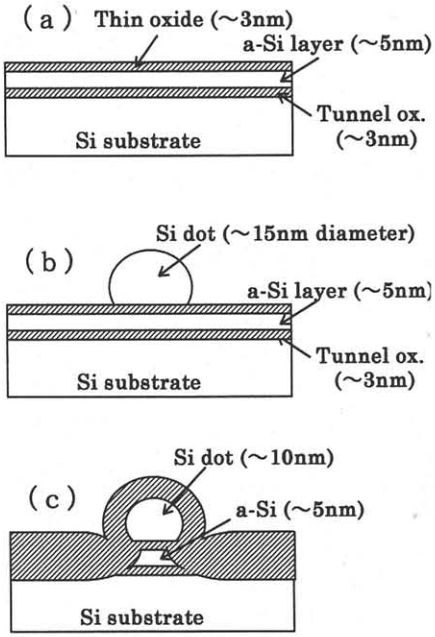

Fig.2 Fabrication method of the Self-aligned double dot memory.

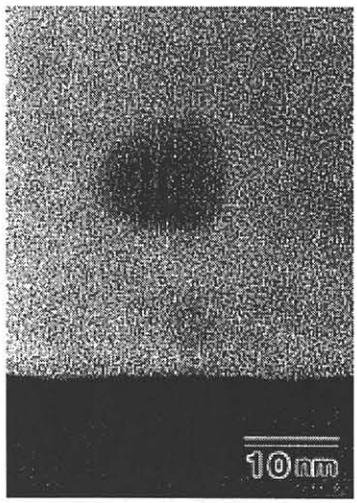

Fig.3 A cross-sectional TEM view of a Si self-aligned double stacked dot structure.

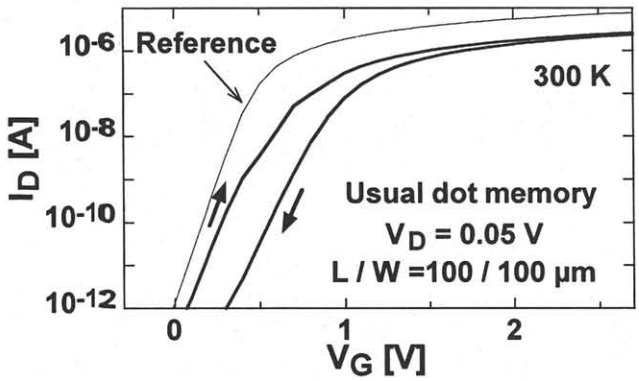

Fig.4 I_D-V_G characteristics for the usual Si dot memory and its reference MOSFET.

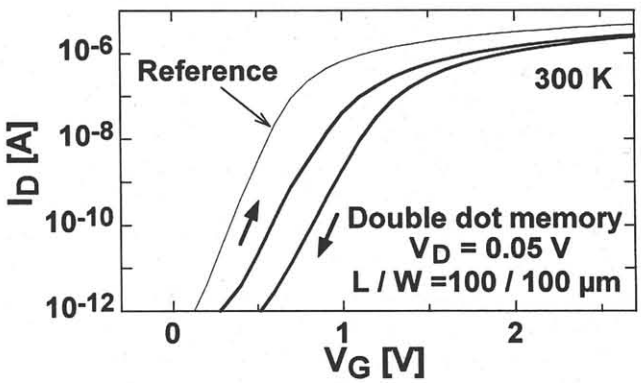

Fig.5 I_D-V_G characteristics for the double dot memory and its reference MOSFET.

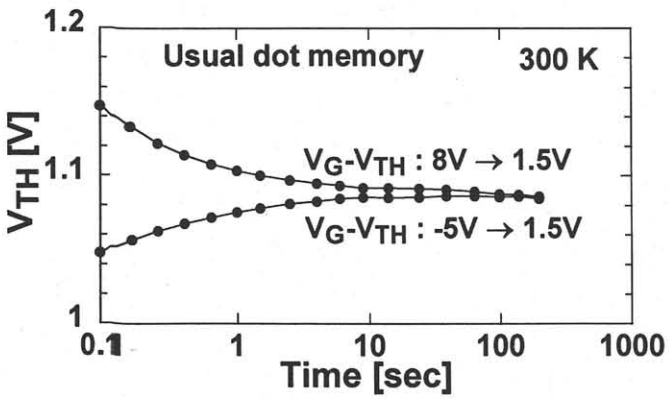

Fig.6 Retention characteristics of the usual single-layer Si dot memory in a inversion region.

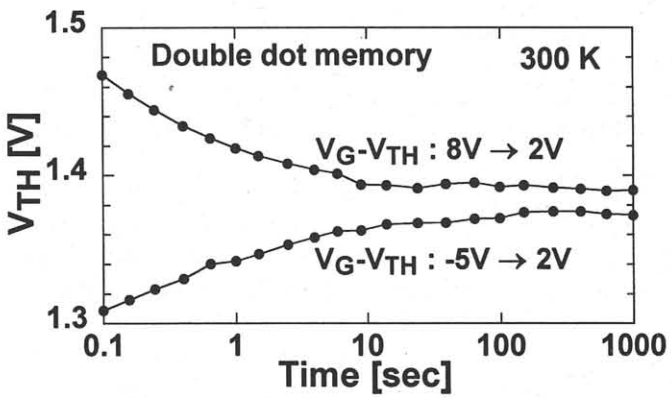

Fig.7 Retention characteristics of the self-aligned double dot memory in a inversion region.