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# Transient Characteristics of Electron Charging in Si-Quantum-Dot Floating Gate MOS Memories

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## 1. Introduction

MOS memory transistors with a silicon nanocrystal floating gate have the multivalued charging capability [1, 2]. We have fabricated MOS structures with a silicon quantum dot (QD) floating gate, and the memory operations have been confirmed at room temperature [3]. A unique hysteresis in the capacitance-voltage (C-V) characteristics and the transient current induced by electron emission from a charged QD floating gate have shown that single electron charging occurs at each of Si quantum dots [3]. This paper describes the memory operation of Si QD floating gate MOSFETs and the multiple-step electron charging to a Si QD floating gate at 300K.

## 2. Fabrication of Si QD floating gate MOSFETs

A single-crystalline Si quantum dot layer was self-assembled on 3.5nm-thick $SiO_2$ by controlling the early stages of LPCVD of pure $SiH_4$ at 610°C [4]. After the first-layer Si dot array formation a ~1nm-thick oxide layer was grown and the second dot layer was deposited under the same conditions. The average dot height and diameter evaluated by AFM were 5 and 10nm, respectively. The total dot density was ~$6\times10^{11}$ $cm^{-2}$. The surface of the second Si dot layer was covered with ~1nm-thick oxide. Subsequently, a 3.3nm-thick amorphous Si layer was grown over the dot layer by LPCVD at 440°C and fully oxidized in dry $O_2$ at 1000°C to form a 7.5nm-thick control oxide. No significant change in the surface morphology was observed in this oxide layer formation. Finally, 200nm-thick $n^+$ poly-Si gate and source/drain junctions were fabricated.

## 3. Results and Discussion

Drain current versus gate voltage ($I_d$-$V_g$) characteristics of a Si QD floating gate MOSFET are shown in Fig. 1. The hysteresis arises from the charging of a Si QD floating gate. The current bumps around 0.3 and 0.8 V indicate that the electron charging to the Si QD floating gate occurs at specific gate voltages. A possible mechanism will be discussed later. As shown in Fig. 2, the drain current versus drain voltage ($I_d$-$V_d$) curves after discharging (solid curves) show apparent negative conductance at $V_g \geq 0.8$ V because partial electron charging to QDs occurs during the measurements at higher $V_g$ as a result of electron tunneling through the 3.5 nm-thick bottom oxide. On the other hand the drain current after charging (dashed curves) is suppressed at low $V_d$, while at higher $V_d$ the drain current increases with increasing $V_d$. This is because electrons stored in the dots near the drain region are extracted to the drain by tunneling through the bottom oxide. Finally, the drain currents after charging coincide with those after discharging at high $V_d$, indicating that the charged states of the Si QD floating gate reach the

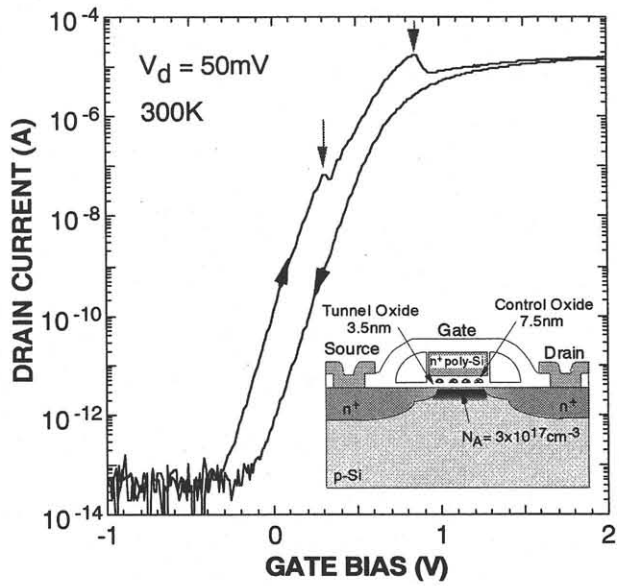


Fig. 1 Drain current-gate voltage characteristics of a Si QD floating gate MOSFET. The gate length and the width are 0.5μm and 10μm, respectively. The gate voltage scan rate was 60 mV/s.

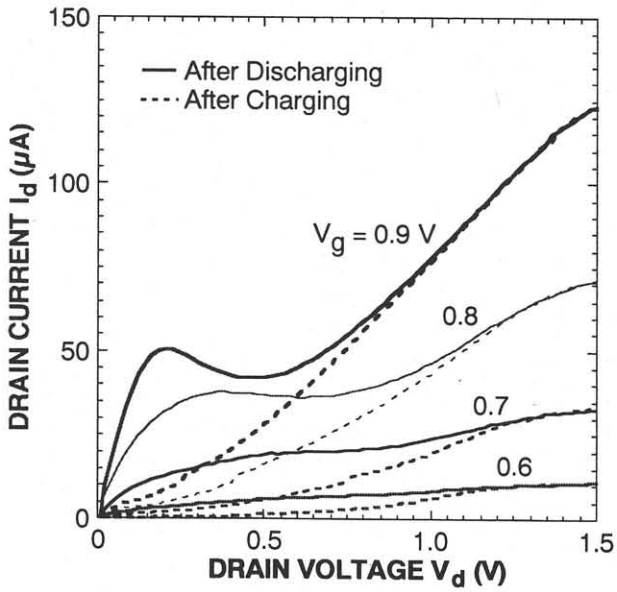


Fig. 2 $I_d$ vs $V_d$ characteristics of a Si QD floating gate MOSFET with a gate length of 0.5 μm.

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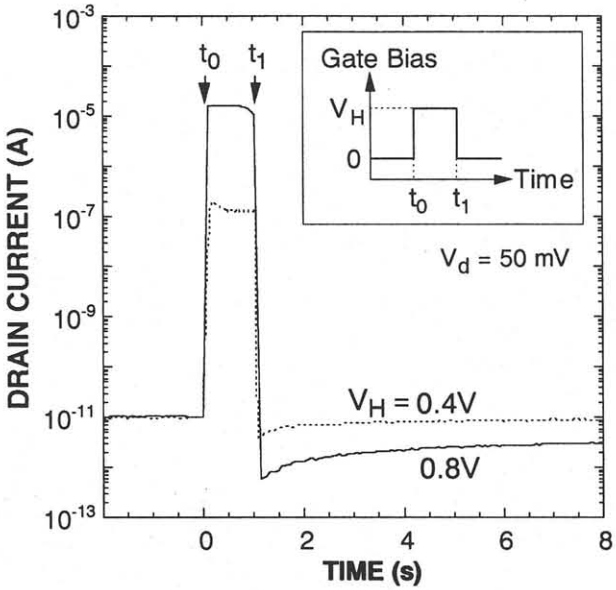


Fig. 3 Temporal change in the drain current of an MOSFET for writing operation by a single-pulse gate bias.

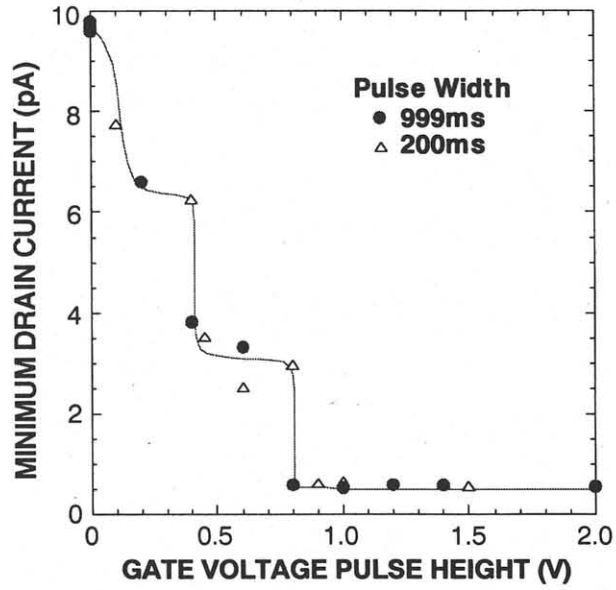


Fig. 4 Minimum drain current at $t = t_1$ as a function of the gate pulse height $V_H$ with different pulse widths.

same steady state.

In order to reveal the charged states of the Si QD floating gate, temporal change in the drain current for a single-pulse gate bias was measured as shown in Fig. 3. The drain current drops to the minimum value at $t = t_1$ and gradually increases to the final steady state. This indicates that a fraction of electrons retained in the dots after writing operation by a positive-pulse gate bias is slowly released at zero gate bias. The minimum drain current at $t = t_1$ is plotted as a function of the gate pulse height $V_H$ as shown in Fig. 4. The stepwise changes in the minimum drain current which occur around 0.2, 0.4 and 0.8 V suggest that the multiple-step electron charging to Si QDs occurs by applying a positive gate pulse, in consistency with the current bumps in the scanned $I_d$-$V_g$ characteristics as shown in Fig. 1. Coulombic interaction among charged quantum dots is thought to cause such multiple-step electron charging. The temporal change in $I_d$ induced by a gate pulse height of $V_H = 0.2$ V from $V_L = -3$ V (erased state) was measured as shown in the inset of Fig. 5. The drain current shows the maximum at $t = t_0$ and decreases due to the electron charging to Si QDs. The maximum drain current corresponds to the discharged (erased) state current at the gate voltage pulse height $V_H$. Thus the discharged state $I_d$-$V_g$ characteristic is obtained as shown by solid circles in Fig. 5. By noting that the threshold voltage shift is about 0.5 V, approximately one electron per dot is stored in a Si QD layer immediately after the writing operation at $V_g \geq 0.8$ V [3].

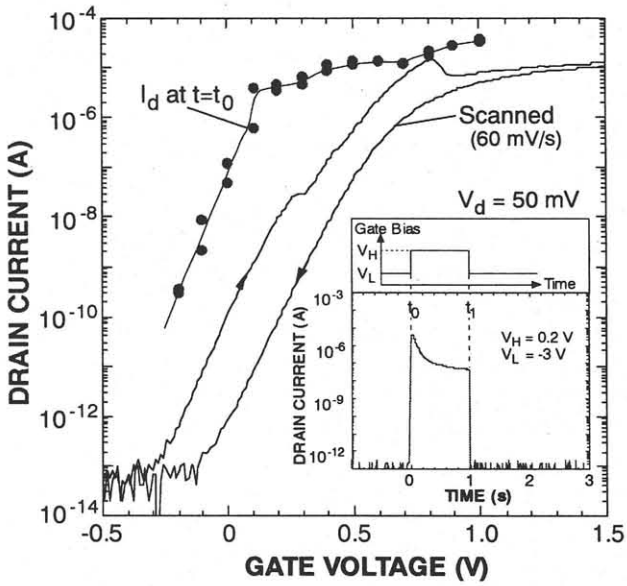


Fig. 5 $I_d$-$V_g$ characteristics after discharging. Temporal change in drain current for gate pulse bias was measured as explained in the inset.

## 4. Conclusion

The memory operation of Si QD floating gate MOSFETs has been demonstrated and the multiple-step charging of QDs to a level of about one electron per dot has been confirmed by the transient drain current measurements.


## Acknowledgment

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