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A Multi-Quantum-Dot Associative Circuit Using Thermal-Noise Assisted Tunneling

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1. Introduction

Single-electron devices have intrinsic difficulties from a viewpoint of system applications: slow operation speed and insufficient reliability [1] due to stochastic tunneling events and serious background charge sensitivity [2]. Thus, the conventional multi-stage digital circuit architecture is not suitable for single-electron devices. New single-electron circuits based on new information processing principles should be invented.

As an example of such circuits, we have proposed circuits using the Coulomb repulsion effect between quantum dots [3], which is described in the next section. This circuit measures the Hamming distance, the number of the unmatched bits between two digital data, which are a core circuit for associative memories. However, this circuit has an intrinsic drawback that is very low operation temperature for practical junction capacitance.

In this paper, we propose a new circuit that can operates at room temperature with practical junction capacitance by using tunneling processes assisted by thermal noise, which is a new operation principle for information processing using quantum structures.

2. Principle of Hamming distance measurement using quantum-dot structures

Let us assume a one-dimensional (1-D) array of quantum dots as shown in Fig. 1, put an electron, e_M, at the center dot D_c, and represent a bit (1 or 0) of the input and stored data by whether an electron is put at each end dot D_e or not. When the corresponding bits of both data are matched, because Coulomb repulsion is symmetric, electron e_M is stabilized at D_c; otherwise it is at one of off-center dots D_o. This bit matching result reflects whether electron e_R tunnels to node N_o. Consequently, electrons whose number is equal to that of the matched bits are accumulated in C_o.

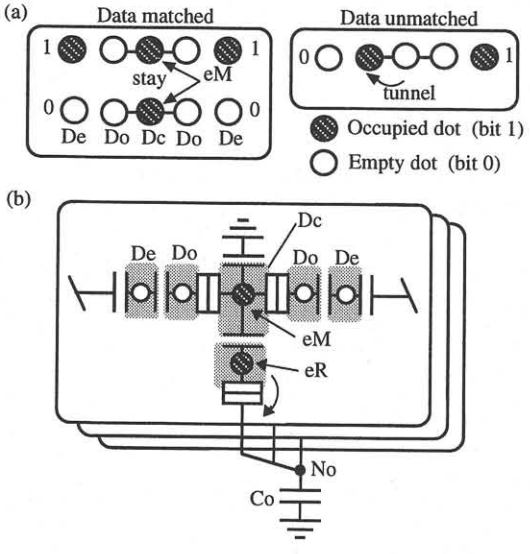

Figure 1: Principle of bit-comparison using Coulomb repulsion effect (a) and bit-comparator circuit (b).

A 3-D arrangement of quantum dots realizing the circuit is shown in Fig. 2. The capacitance C_o corresponds to the gate capacitance of an ultrasmall CMOS transistor.

However, in this circuit, because the charging energy is directly related to the tunnel junction capacitance (C_j), very low C_j (0.01 aF) is required for room temperature operation. This value is very difficult to realize.

3. A multi-quantum-dot circuit using thermal-noise assisted tunneling

We propose a new circuit and structure using tunneling processes assisted by thermal noise. In the new circuit, additional dots are inserted between D_c and D_o, and between D_c and N_o as shown in Fig. 3. By applying appropriate bias voltages, the profile of the total energy of the 1-D dot array structure $(D_e, D_o, \cdots, D_c, \cdots, D_o, D_e)$ has two peaks at the additional dots, and has minimal values at D_c and both of D_o as shown in Fig. 4. For *1-1 state*, where electrons are put at both D_e, the energy at D_o rises up, thus e_M is most strongly stabilized at the center position. Therefore, the difference between *0-0 state* and *0-1(or 1-0) state* has to be considered.

4. Circuit simulation results

We analyzed the proposed circuit shown in Fig. 3 by Monte Carlo single-electron simulation, where the tunnel junction capacitance is 0.1 aF; tunnel resistance R_t is 5 MΩ; operation temperature is 300K.

Figure 5 shows the total energy as a function of the position of e_M. The energy barrier height for e_M at D_c is larger than the thermal energy at room temperature.

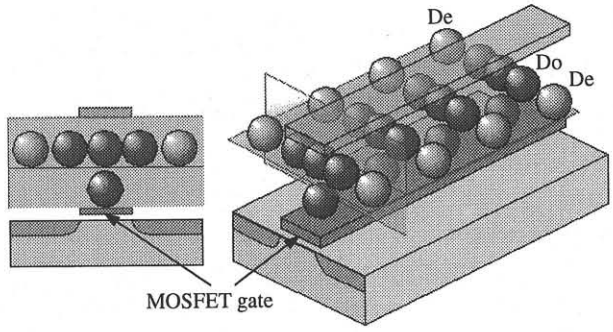

Figure 2: Quantum dot structure.

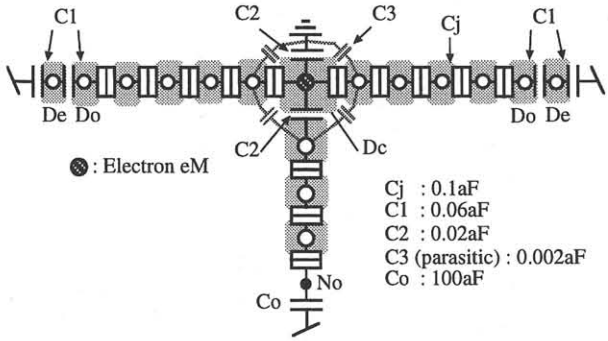

Figure 3: A multi-quantum-dot circuit.

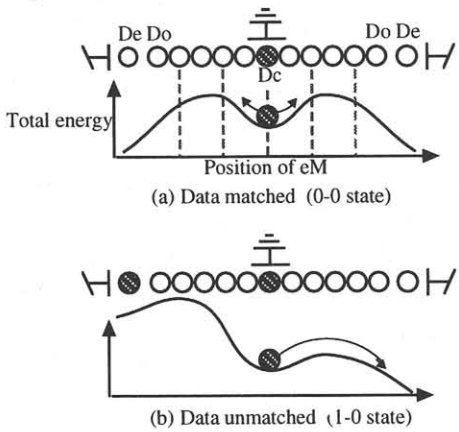

Figure 4: Total energy profile of 1-D dot-array structure.

Because this energy barrier height in *0-1(1-0) states* is lower than that in *0-0 state*, there exists a certain time span t_0 within which e_M in *0-1(1-0) states* moves to D_o due to thermal noise, while e_M in *0-0 state* stays at the center position. Figure 6 shows the relation between operation temperature and time when e_M moves to D_o. At room temperature (300K), t_0 is about 1 μs. However, t_0 depends on R_t.

Figure 7 shows time dependence of the voltage at N_o as a function of the Hamming distance at room temperature, where the voltage for a distance of 0 bit was considered to be 0 V. The voltage changes are proportional to the Hamming distance, and larger than 1 mV, which is large enough to detect with an MOSFET. Thus, it was confirmed that the new circuit can operate at room temperature for the junction capacitance 10 times larger than that in the previously proposed circuit.

5. Conclusion

A new operation principle and multi-quantum-dot circuit using thermal noise were proposed. This operation principle seems to be similar to phenomena called "stochastic resonance". In this circuit, the operation speed is determined by the tunneling resistance and operation temperature. The multi-quantum dot structures will be realized by using well-controlled self-organization fabrication technologies.

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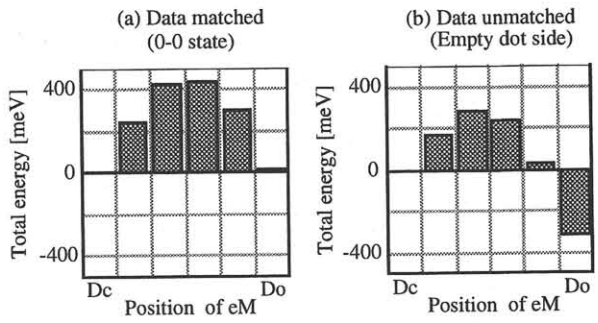

Figure 5: Relative total energy changes of 1-D dot array structure.

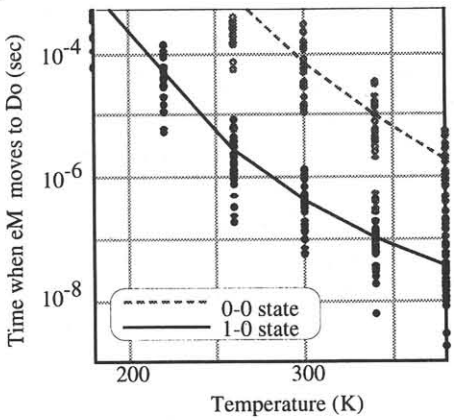

Figure 6: Relation between operation temperature and time when e_M moves to D_o.

References

[1] S. Shimano, et al., *Jpn. J. Appl. Phys.*, **38**, 403 (1999).
[2] R. H. Chen, et al., *Appl. Phys. Lett.*, **68**, 1954 (1996).
[3] T. Morie, et al., *Superlattices & Microstructures*, in press.

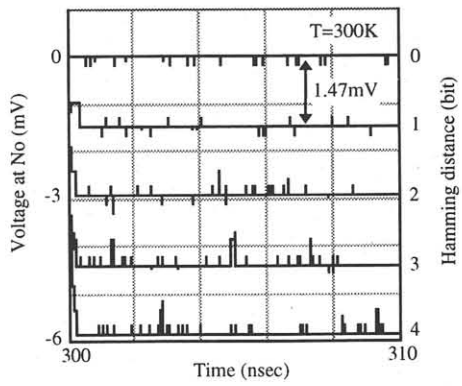

Figure 7: Time dependence of the voltage at N_o as a function of the Hamming distance.