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Novel Single Electron Memory Device Using Metal Nano-Dots and Schottky In-Plane Gate Quantum Wire Transistors

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1. Device Structure and Operation Principle

Single electron memory device is a one of the promising key device for future quantum integrated circuits because of its high memory density and extremely low power operation. Most of the previously reported single electron memory devices utilize small embedded semiconductor dots (mostly Si dots)[1,2]whose position and size are difficult to control.

In this paper, we report on successful realization of a novel single electron memory device utilizing Schottky in-plane gate (IPG) quantum wire transistor (QWTr) having nano-Schottky metal dots whose position and size can be precisely controlled. The device structure is shown in **Fig.1(a)** which was proposed by the present authors[3].

In this device, zero-th and first quantized conductance step of the Schottky IPG QWTr is switched by Coulomb charging of the metal nano-dots placed on the top as schematically shown in **Fig.1(b).** Charging of the metal nano-dot is achieved by Coulomb blockade type electron tunneling by applying a bias between the charging control gate. The surface potential change due to dot charging causes potential modulation in the quantum wire, and switches the 1D channel on and off. According to the preliminary computer simulation of this device structure, switching of the quantized conductance can be obtained by only a few electron charging to the each Pt dot having the size of 20nm.

2. Device Fabrication

The Schottky IPG QWTr for the memory switching was fabricated on an AlGaAs/GaAs quasi 1D etched wire which was formed by electron beam (EB) lithography and chemical etching on an MBE grown quantum well (QW) wafer. The Schottky IPG electrodes were formed by in-situ electrochemical process using the set-up shown in **Fig.2(a)**. Here, both pulse etching of the GaAs surface and IPG metal deposition can be done in the same electrolyte.

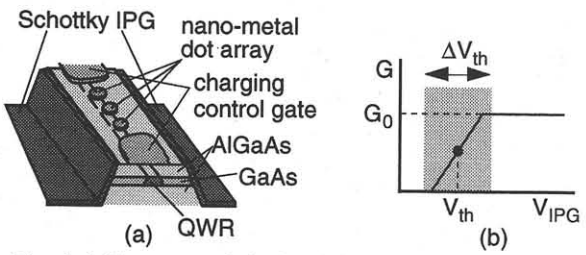

Fig. 1 (a)Structure of single electron memory device, and (b) operation principle.

3. Device Characterization and Performance

Top Gate Control of Schottky IPG QWTr

To investigate whether the IPG QWTr can be controlled by surface potential change at the top, Schottky IPG QWTr having a simple top bar gate instead of metal nano-dots was fabricated and tested. As shown in **Fig.3(a)**, systematic shifts of the threshold of QWTr, $V_{TH,IPG}$ with change of the top gate bias V_{TG} were observed in the quantized conductance characteristics. As shown in **Fig.3(b)**, the transfer ratio of V_{TG} change to $V_{TH,IPG}$ change was almost as large as unity. Thus, efficient threshold control can be made by the top metal gate.

Size- and position-controlled deposition of the Pt dot used as the memory node on top of QWTr was achieved also by the in-situ electrochemical process in combination with EB lithography. **Figure 2(b)** shows an SEM image of fabricated nano metal dot having tunnel

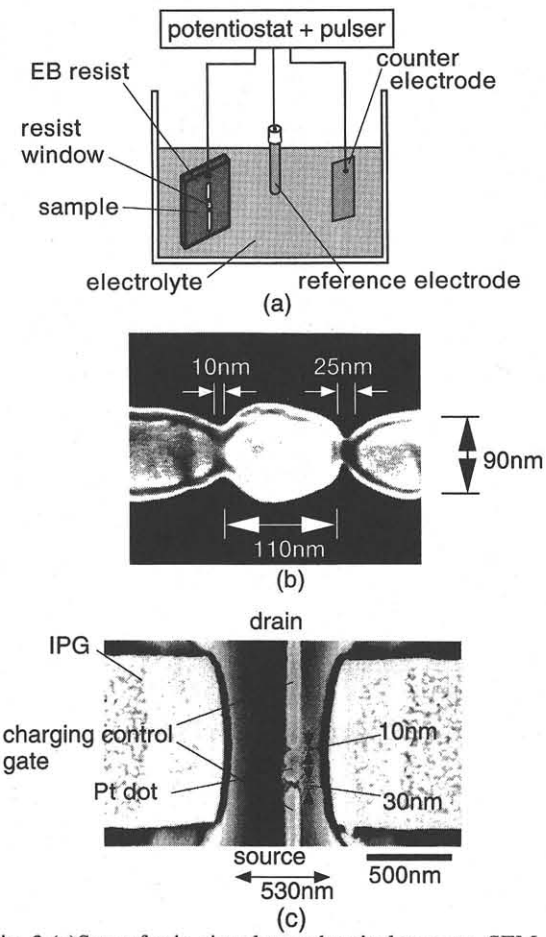

Fig. 2 (a)Setup for in-situ electrochemical process. SEM image of (b)Pt dot with charging control electrode, and (c)single electron memory device.

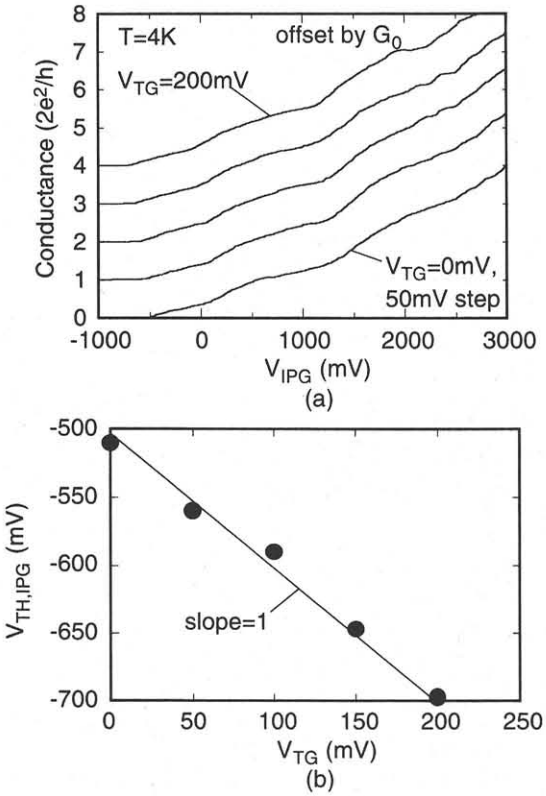

Fig.3 (a)Conductance characteristics of top bar gate QWTr, and (b) threshold shift by top bar gate control.

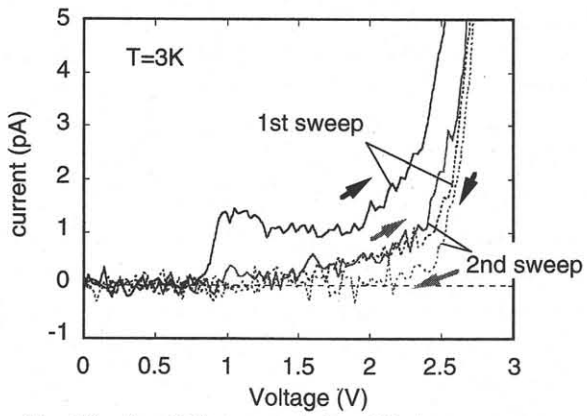

Fig. 4 In-plane I-V characteristics of Pt dot structure.

barrier of 10-25nm. Single electron memory device having nano metal dot was successfully fabricated as shown in **Fig.2(c)**. A Pt dot with tunnel barrier of 10-30nm on both side was formed on the IPG QWTr.

Charging Characteristics of Metal Nano-Dots

The Pt nano-dots showed well-behaved Schottky I-V characteristics on GaAs as confirmed directly by a conductive AFM tip. The measured in-plane I-V characteristics of the fabricated nano-Pt dot structure shown in **Fig.2(b)** are shown in **Fig.4**. We observed clear hysteresis. Similar characteristics was also observed in negative voltage sweep. The hysteresis vanished at second positive voltage sweep, however, it appeared again after giving a negative voltage sweep and coming back, and vice versa. This hysteresis behavior was maintained at least up to 130K.

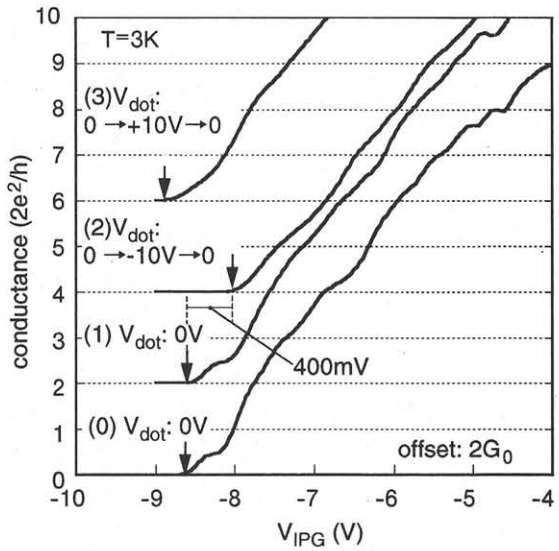

Fig.5 Conductance characteristics of single electron memory device.

Observed I-V characteristics can be explained by the charging of the Pt dot caused by tunneling current transport through two asymmetric tunnel barriers. Tunneling barriers in between the Pt dot and electrode should be GaAs rather than air gap and barriers are inevitably asymmetric. According to a basic tunnel current calculation of this system, transition from direct tunneling to Fowler-Nordheim tunneling is expected to take place at the thicker tunnel barrier than the thinner one, producing large conductance asymmetry. Then, current continuity under such asymmetric tunnel conductance can only achieved by self-adjustment of the dot potential through self-charging of the dot.

Memory Device Operation

The fabricated memory device showed clear pinch-off with conductance steps as shown in **Fig.5**. This characteristics was reproducible. After the application of −10V to the charging control electrode, clear threshold shift towards positive IPG bias was observed. In contrast, after application of +10V to the charging control gate, negative threshold shift was clearly seen. Thus, memory device operation was successfully demonstrated.

A simple estimate shows the numbers of stored electrons is several ten to hundred in our device. However, this electron number can be reduced by further reduction of the Pt dot size.

References

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