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Superlattice- and Ultrashort-Channel Field Effect Transistors Fabricated by Cleaved Edge Overgrowth

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We study high mobility electrons in the presence of ultra short period periodic potentials of different strengths. We find striking signs of the artificial bandstructure, which are clearly manifest in DC and magnetotransport measurements. The relevance of high mobility miniband transport to Bloch oscillations is discussed. Further we investigate ballistic DC transport in ultra short channel vertical field effect transistors and demonstrate the influence of different potential landscapes imposed on the channel.

For the present studies we have developed a novel vertical HIGFET (heterostructure insulated gate field effect transistor), which is grown by two subsequent MBE steps using the *cleaved edge overgrowth* technique [1]. This technique has the beauty that all relevant features of the devices can be defined to atomic precision. For our particular devices the first growth occurs on a (001) semi-insulating GaAs substrate and comprises two n+ GaAs contact layers (source and drain), between which a barrier is inserted. This barrier can either be a GaAs/AlGaAs superlattice, a single AlGaAs layer, or a p+ delta doped GaAs layer. The sample is then cleaved while still in the ultra high vacuum chamber, and immediately after overgrown in (110) direction by a second layer sequence. This second growth step comprises a GaAs quantum well, in which the electronic transport will take place, an AlAs gate barrier and the gate, which can be either n+ GaAs or metallic Al. The resulting device represents a vertical field effect transistor, the channel length and thickness of which are defined by MBE growth, and the transport in which occurs at an atomically smooth interface.

We first concentrate on devices where the electronic transport is governed by a two dimensional electron gas under the influence of a 15 nm period GaAs/AlGaAs superlattice. The magnitude of this influence can be tuned by varying the quantum well thickness, in the limit of zero quantum well thickness the two dimensional electron gas resides entirely in the superlattice. All experiments are performed at liquid helium temperatures. Magnetotransport experiments are used to determine the range of available electron densities, to estimate the electron mobility and to determine the Fermiology of the artificial bandstructure [2]. As an example we find that the electron density can be tuned between 5e11 cm^-2 and depletion, and in weakly modulated systems for densities even below 1e11 cm^-2 the fractional quantum hall effect is well developed, which hints to electron mobilities above 1e6 cm^2/Vs. The transistor characteristics exhibit a region of negative differential resistance at low source-drain voltages. We attribute this negative differential resistance to electron localization due to Bloch oscillations. The electric field at peak current of 167 V/cm is the lowest reported so far, indicating a remarkably long scattering time [3]. We observe that the peak-to-valley ratio of the negative differential resistance decreases with increasing quantum well thickness, corresponding to weaker modulation strengths, while at the same time the saturation current increases. This is consistent with the model of an artificial bandstructure generated by the periodic potential modulation through the superlattice. A closer look at the transistor characteristics for different electron densities reveals features which may be related to Bloch-phonon resonances.

In the second part of the talk we will present results that are obtained in our effort to test the limits encountered towards ultra-short channel transistors. Our experiments are for now steered towards fundamental research, and are performed at low temperatures. The sample design is similar to the above described superlattice field effect transistors, except that here the superlattice is replaced by a single barrier, the thickness of which then determines the channel length. All devices are normally off. We investigate devices with channel lengths of 50 nm and below. Device characteristics of transistors with different channel designs are compared.

References:

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