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# Memory Operation of InAs Quantum Dot Field Effect Transistor

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## 1. Introduction

InAs quantum dots (QDs) have received much attention because of their importance in both electrical and optical device applications. Subband transition in embedded InAs QDs gives a possibility of a long wavelength photodetector [1]. Recently, InAs QDs are introduced to store charge and function as memory device [2]. In recent researches, InAs QDs are embedded in heterojunction structures [3, 4]. The vertical transport structures reportedly have a clear memory effect of InAs QDs but also have the application limit with the general devices. In this study, we investigated the InAs QDs memory effect in a conventional lateral transported high electron mobility transistor structure, which leads to a room temperature operation and can adopt the conventional circuit concepts. Heterostructure could provide high speed channel for carrier supply and QD structure plays a role of a memory.

## 2. Experiment and results

In this experiments, InAs QDs are grown by the self-assembled method – S-K growth mode. The sample is prepared on semi-insulating GaAs substrate and 5 stacks of QD layers are grown by MBE. Then GaAs and AlGaAs barrier layers are added on the QD layers. Figure 1 shows the proposed structure. Gate length is 2μm and the width is 50μm.

Figure 2 shows the PL data of the grown QD sample. From 10μm peak position, we could define the InAs QDs in this structure. Figure 3 also shows the AFM image of a QD layer. The QD density of one layer is estimated to $3\times10^{10}$ $cm^{-2}$.

Figure 4 shows the hysteresis of $I_{DS}$-$V_{GS}$ characteristics of the proposed structure. After the charging process with the positive gate bias, large difference of drain current is exhibited. This comes from the stored carriers in QDs layer, which are located near 2-D electron channel.

Between gate and source, the carriers of 2-D electron channel and QD are affected by the gate control bias, simultaneously. Thus the parallel connection of capacitors can be established and the total capacitance equation is expressed as follows;

$$C_G = C_0 // (C_{ch} + C_{QD}) = \frac{1}{\frac{1}{C_0} + \frac{1}{C_{ch} + C_{QD}}} \quad (1)$$

where $C_G$ is the total capacitance of gate to source and $C_0$ is the capacitance of the n-AlGaAs depletion region.

In Figure 5, we did the capacitance-voltage (CV) measurement at low frequency–10KHz. The small figures in Fig. 5 show the capacitors model of the proposed structure, Fig. 1. At low frequency range, the QD can respond to the AC signal. Thus the relatively slow response of QD than that of 2-D electron channel could be shown in the C-V hysteresis graph, Fig. 3. At the first step, $C_{ch}$ and $C_{QD}$ are almost zero because of a full depletion in the channel and the QD region by the negative gate bias, so $C_G$ goes to zero by equation (1). In the positive direction of gate bias sweep, carriers are supplied by the fast 2-D electron channel current and the total capacitance is increased by the increase of $C_{ch}$ and $C_{QD}$. In the reverse sweep, the total capacitance $C_G$ is decreased by amount of the carrier difference in QD. The carriers in QD has a slow discharging time than 2-D electron channel, in reverse sweep, the capacitance of QD has a value of $C_{QD}'$, which is smaller than the value of $C_{QD}$ in positive sweep. This capacitance difference is memory effect of QD.

We confirmed this result by comparing the CV measurement results in various frequency ranges. In the low frequency range, the similar tendency is shown. As the measurement frequency increased to higher range, the hysteresis is disappeared. This is because carriers in QDs cannot fully respond to the high frequency signal. Thus $C_{QD}$ can be neglected in the total capacitance and one can see the series connection of the depletion capacitance and 2-D electron channel capacitance.

## 3. Conclusions

Memory operation of InAs QD FET is presented. From the PL data, one can understand InAs QD existence and the density of QDs can be estimated from AFM image. The lateral transport occurs through the parallel connection of 2-D channel and QD layers. It is shown that carrier storage of QD through lateral injection by the current hysteresis and CV measurement.

## References

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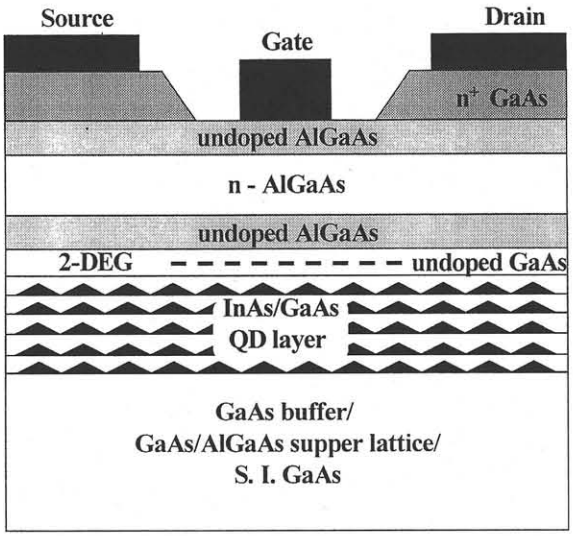


Figure 1. The structure of quantum dot heterojunction field effect transistor.

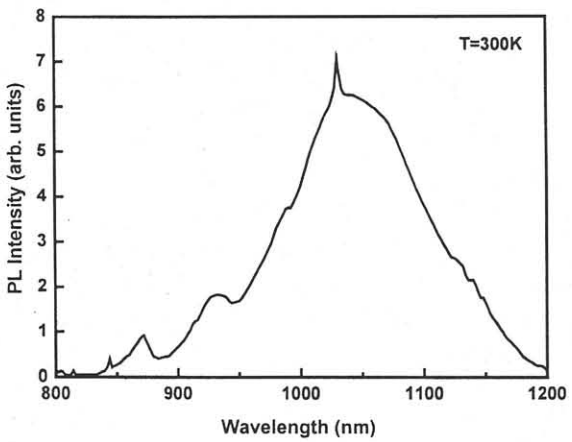


Figure 2. Photoluminescence data of MBE grown self-assembled InAs QD. The 10 mW pump Ar laser is used in the Measurement.

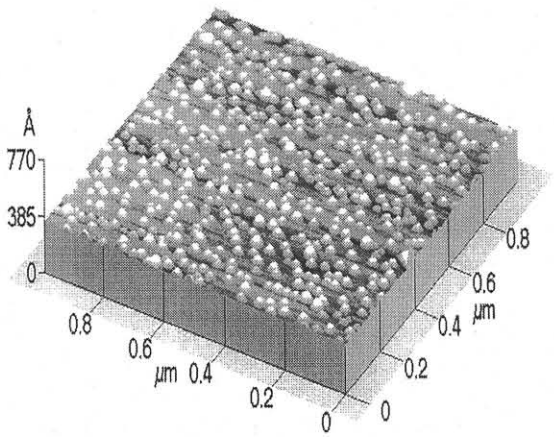


Figure 3. AFM image of InAs QD. The density is about $3\times10^{10}$ $cm^{-2}$. The diameter and height are estimated to 300 Å and 55 Å.

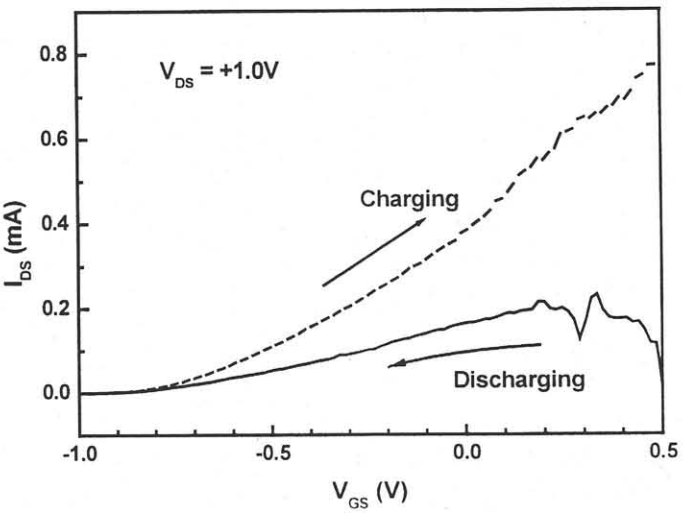


Figure 4. Current hysteresis of the proposed structure at 300 K. After the charging process, large reduction of drain current is revealed.

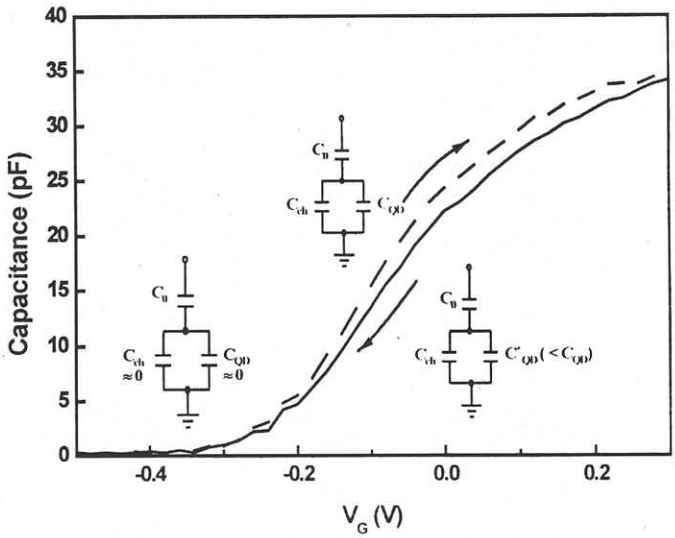


Figure 5. The model is coincide with the measured C-V curve at 10 KHz frequency. Dashed line is positive sweep direction of gate bias and solid line is the reverse sweep. (This result is done with the C-V measurement pattern, 100 μm × 100 μm square)