Extended Abstracts of the 2000 International Conference on Solid State Devices and Materials, Sendai, 2000, pp. 352-353

E-3-1 (Invited)

Fingerprint Identification System on a Single Chip Based on Advanced Circuit and Device Technologies

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Introduction

The key technologies for a System on a Chip (SoC) are an algorithm (software) that handles system functions, a circuit that executes the algorithm, and a device that provides the circuits. In order to produce an actual system on a single chip, an optimized chip architecture that unites these key technologies is strongly required. This paper considers a single-chip fingerprint sensor/identifier [1] as an example of a SoC and describes the optimization of the identification algorithm, circuit design, and device structure.

Chip Architecture

A fingerprint sensor should be as large as a finger because it senses the fingerprint of a finger in contact with the chip. A high-performance processor and large memory are required for fingerprint identification. Integrating these elements in a single chip brings normally results in a large chip area. This problem is solved by introducing a chip architecture in which the processor has a pixel-parallel structure and the sensor element is stacked directly above the circuits in each pixel (Fig. 1). A fingerprint image is produced by measurement of the capacitance (Cfr,Cfv) between the finger surface and sensor plate. Then, the pixel-parallel processor directly under the sensor plate compares the sensed image with the user template. This architecture achieves fast and efficient sensing and identification.

Algorithm

We adopt the fingerprint identification method based on pattern matching of fingerprint images [2]. For registration, an image of the user's fingerprint is thinned down and registered in the chip as a user template. For identification, a sensed fingerprint is authenticated by means of pattern matching between the sensed and template images. This algorithm is based on image processing. Thus, it is the most suitable algorithm for the pixel-parallel processor.

Circuit Design

Pattern matching requires a large amount of calculation. In order to execute the algorithm in practice, the pixel-parallel processor has to be able to quickly compare fingerprint images without consuming a lot of power. This is accomplished by using the structure shown in Figs. 2 and 3 [3]. The pixel comprises a memory that stores the user template, a sensing circuit that senses and binarizes a fingerprint, and a processing circuit that compares fingerprint images. Each pixel is connected to neighboring pixels and shifts the sensed image to compensate for variation of finger position. The totaling of the results from all pixels, which consumes the most time in pattern matching, is performed by the variable-delay circuit (VDC) [3] contained in each pixel. The delay of a VDC depends on the comparison result and all VDCs are connected serially. The measurement of the delay of this VDC chain can total the results from all pixels with only one pulse. Thus, the high-speed, low-power totaling and identification are achieved.

The sensing circuit has to prevent the influence of the large parasitic capacitance Cp of the sensor plate caused by making the plate directly above the circuits. For this purpose, the sensing circuit shown in Fig. 4 was developed [4]. This circuit uses a differential amplifier with a reference capacitance $Cref$ that is equivalent to the sum of Cp, and can reduce the influence of the parasitic capacitance. It also achieves high sensitivity by incorporating a charge-transfer amplifier [4].

Device

A solid-state fingerprint sensor is vulnerable to electrostatic discharge (ESD) as well as physical and chemical damage due to repeated direct finger contact with the chip. A new device structure is proposed to prevent such damage [5]. Each sensor plate is surrounded by a lattice-like wall that is exposed at the chip and connected to the ground. This wall can discharge the charge of a finger (Fig. 5). The chip surface is coated with a hard film to protect the sensor and the circuits. This structure significantly improves sensor and circuit reliability.

Implementation and Results

To check the effectiveness of the proposed architecture, we fabricated a test chip using standard 0.5-μm CMOS/sensor processes (Fig. 6). It was confirmed that the sensed image can be used for identification. The SEM micrographs in Fig. 7 clearly show that the sensor plate and GND wall are built above the circuits and each pixel is surrounded by the GND wall. The high reliability of the sensor and circuits was demonstrated by a tapping test (1 MPa pressure, 10^4 times) and an ESD test (±2 kV direct contact charging) [5].

Conclusion

A single-chip fingerprint sensor/identifier has been described as an example of a System on a Chip (SoC). This first-ever fingerprint identification system on a single chip was achieved by improvements in algorithm, circuit-design and device technologies, as summarized in Fig. 8. Nowadays, design technology is generally moving forwards SoC. However, to realize an actual SoC which contains from a processor to a human interface requires not only excellence of each technology but also unit of all technologies. Therefore, the key technologies working in harmony is the most important thing. This approach represents one of the directions of future SoC technology.

Acknowledgements

The authors thank K. Takeya, J. Yamada, R. Kasai, S. Konaka for their encouragement and support. They also thank K. Kudou, M. Yano, T. Kumasaki and T. Adachi for the fabrication and measurement.

References

[1] S.Shigematsu et al., *IEEE J. Solid-State Circuits*, **12** (1999) 1852
[2] T. Kobayashi et al., *Proc. 4th Int. Conf. Computing and Information*, (1992) 341
[3] S. Shigematsu et al., *Proc. ASIC/SOC Conf.*, (1999) 310
[4] H. Morimura et al., *IEEE J. Solid-State Circuits*, **5** (2000) 724
[5] K. Machida et al., *IEDM Tech. Dig.*, (1999) 887

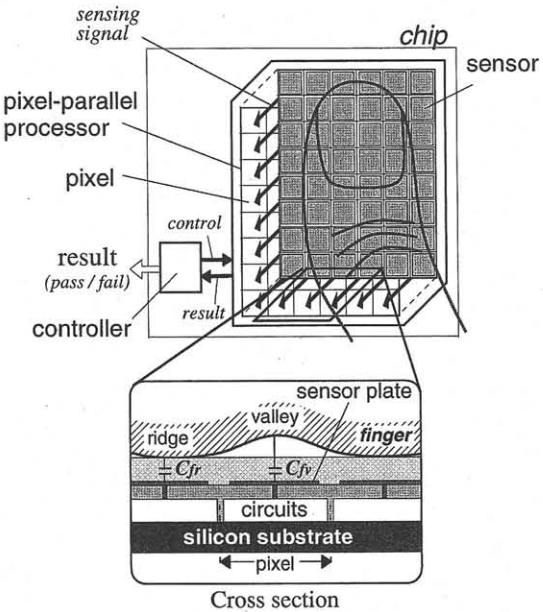


Fig. 1 Architecture of the fingerprint identification chip.

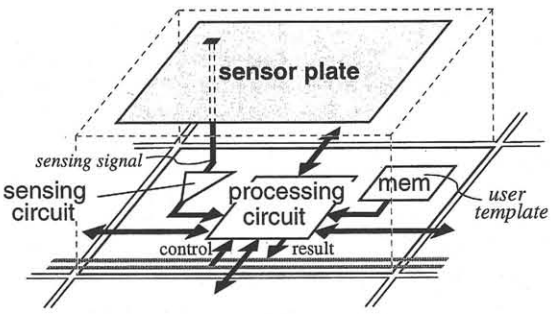


Fig. 2 Basic pixel concept.

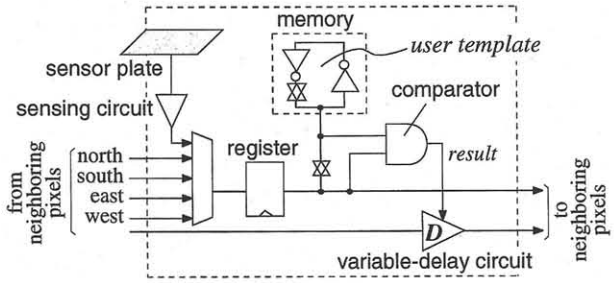


Fig. 3 Circuit diagram of a pixel.

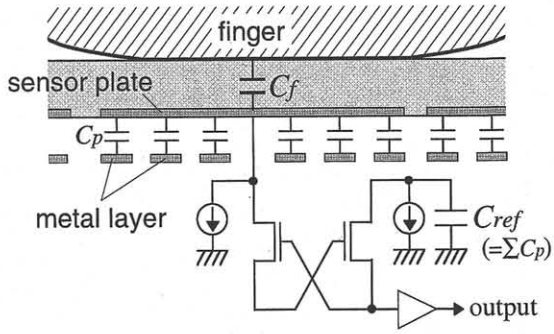


Fig. 4 Sensing circuit scheme.

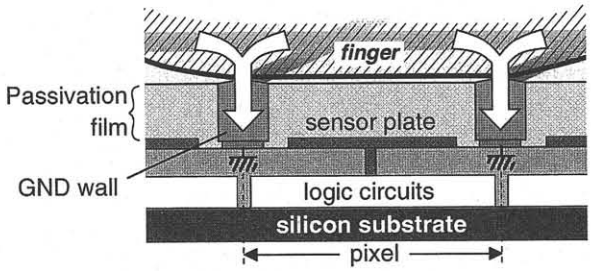
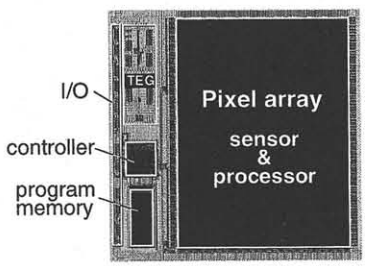


Fig. 5 Discharging path with GND wall.



Process	0.5-μm stand. CMOS, 3-metal, sensor proc.
Die size	15 mm x 15 mm
pixel array area	10.1 mm x 13.5 mm
no. pixels	20,584 (124 x 166)
density	311.3 dpi
Tr. count	3252 K
Pixel size	81.6 μm x 81.6 μm
Tr. count	158
Time & Energy (per image)	
sense/binarize	2 ms , 6.2 mJ
identify	100 ms , 2.6 mJ
Supply voltage	3.3 V

Fig. 6 Test chip.

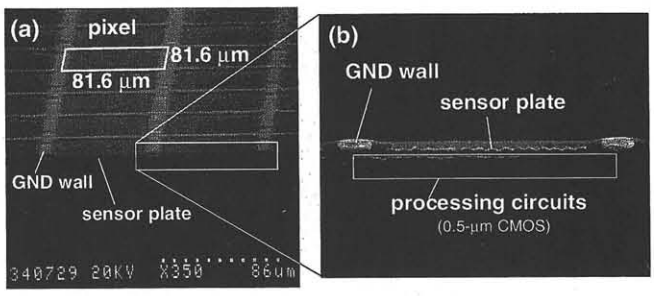


Fig. 7 SEM micrograph: (a) pixel array, (b) cross section of the pixel.

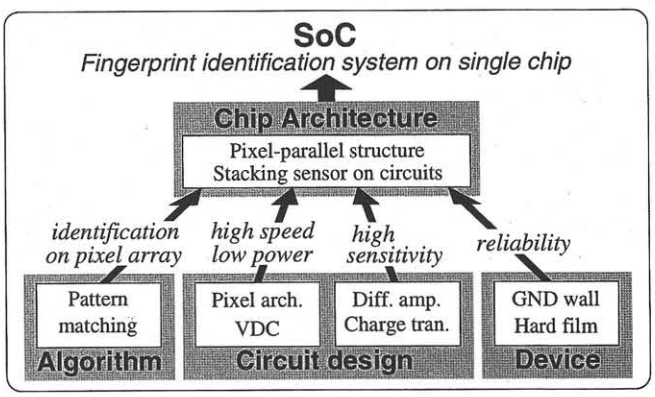


Fig. 8 Approach to actual SoC.