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A Stacked-CMOS LSI Architecture for Reducing Operation Voltage and Current

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Abstracts

We propose a Stacked-CMOS architecture to efficiently use low-breakdown-voltage advanced CMOS under high system supply voltage. The architecture provides vertically divided voltages to stacked plural CMOS circuits and reduces operation current in charge-recycling manner. Test elements using new voltage dividers were fabricated with the 0.20 μm CMOS/SIMOX process. Fluctuation of the applied voltages to each CMOS block was reduced to 10% with the power penalty of only 6 mW.

1. Introduction

Lowering supply voltage is an effective way of reducing LSI power consumption. However, doing so enlarges the difference between the voltage used in LSIs and that supplied from systems, 3.3 or 5.0 V, resulting in the need for high-cost components in modules. One solution is an on-chip converter [1]; however, on-chip converters require external inductors and capacitors and have difficulty handling large currents, e.g. 250 mA. On the other hand, charge-recycled CMOS circuits have been proposed for DRAM [2] and bus architecture [3]. In these architectures, the currents flowing through each divided circuit are equal. Here, we propose a Stacked-CMOS architecture that can be applied to random logic.

2. Architecture

Figure 1 shows schematics of the Stacked-CMOS architecture and the conventional down-converter architecture with a switching regulator. In the Stacked-CMOS architecture, the CMOS random logic is divided into plural low-voltage circuit blocks that are vertically stacked between V_{DD} and V_{SS}. Voltage V_{int} of the common power line is managed by the voltage divider between V_{DD} and V_{SS}. The advantage of the Stacked-CMOS architecture is that it uses one-*m*th the current of the down-converter architecture because the lower block can recycle the current that has flowed through the upper block. Figure 2 shows the efficiency versus load current of the Stacked-CMOS and down-converter architectures. The efficiency of the converter architecture decreases as the load current is increased. This is because the voltage converter supplies the whole load current through output transistors, and, as a result, the power loss by the on-resistance of the transistors increases. On the other hand, there is no decrease in the efficiency even at high load current because core circuits can use the current directly from system's power-supply.

In addition, the switching regulator needs a large external inductor and capacitor. The Stacked-CMOS architecture eliminates these parts; it only needs internal voltage divider circuits.

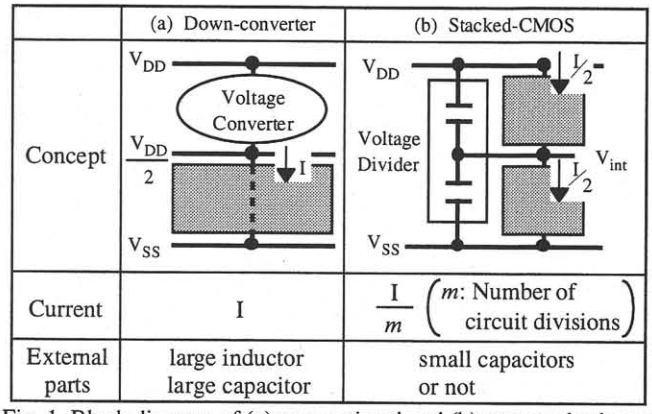

Fig. 1. Block diagram of (a) conventional and (b) proposed schemes.

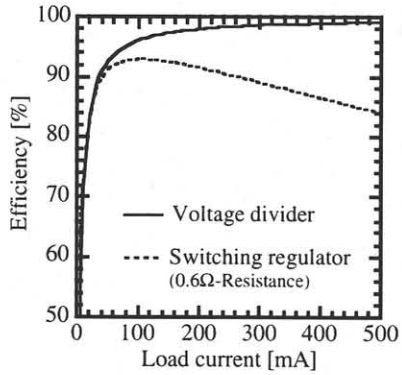

Fig. 2. Comparison of circuit efficiency with the switching regulator and voltage divider.

3. Voltage Dividers

In ref. [2], only series capacitors were used for the voltage divider [see Fig. 1(b)], which keeps the intermediate voltage V_{int}. However, the series capacitor type voltage divider can not hold the V_{int} when the difference between the upper and lower block current becomes large because the fluctuation of V_{int} is simply proportional to the ratio of the current difference.

$$\Delta V_{int} = \frac{\int I_{upper}\,(1 - I_{lower}/I_{upper})\,dt}{C} \qquad (1)$$

In order to apply the Stacked-CMOS architecture to random logic, we propose two types of divider circuit for the voltage divider: a MOS-diode type and a comparator type with a current driver. Figures 3(a) and (b) show these dividers in the case of two intermediate voltages.

In the MOS-diode type, part of the excess/deficient current for the lower circuit flows through the added MOS diodes, which stabilizes the V_{int}. However, the effect depends on the amount of core circuit current.

In the comparator type, both the PMOS and NMOS are set at the off-state when the fluctuation of V_{int} is smaller than the

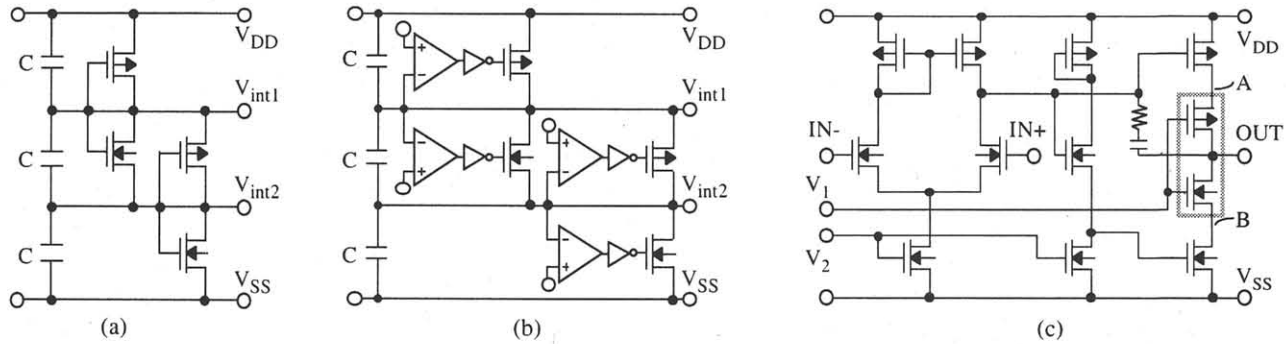

Fig. 3. The voltage dividers with two intermediate voltages; (a) MOS diodes, (b) comparators with current driver, (c) circuit diagrams of the operational amplifier including the modified output stage.

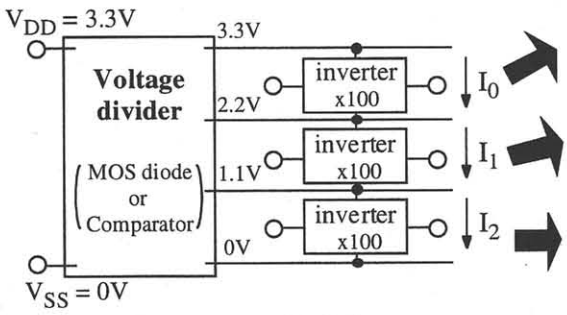

Fig. 4. Test element block diagram.

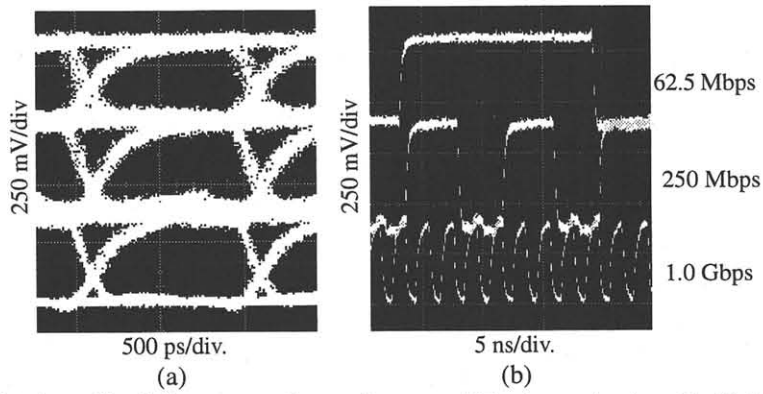

Fig. 5. Output waveforms of upper, middle, lower circuits with 50 Ω termination. (a) Eye patterns at 1.0 Gbps operation. (b) Outputs at 62.5 Mbps (upper), 250 Mbps (middle), and 1 Gbps (lower) circuit operation.

setup value, e.g. 0.1 V. The intermediate-voltage power line is connected to the minus inputs of the two comparators. The negative outputs of the comparators are connected to the gate of the MOSFETs. The comparator circuit was modified for operation at the supply voltage. The voltage applied to all MOSFETs is kept below the breakdown voltage by adding two transistors to the output stage to clamp the voltages of nodes 'A' and 'B' [Fig. 3(c)]. The applied voltages to the PMOSs and NMOSs are 2.5 and 2.0 V respectively.

4. Experimental Results and Discussion

Test elements were fabricated using the 0.20 μm CMOS/SIMOX process. The SOI isolation provided a simple layout of 100-stage inverter-gate chains for the upper, middle, and lower block circuits [Fig. 4]. The external supply voltage of 3.3 V was divided into three parts using the voltage divider so that the internal voltages were set at 2.2 and 1.1 V.

After confirming eye opening in the stacked circuits' outputs at 1-Gbps simultaneous operation (Fig. 5), the fluctuation of the V_{int2} versus the ratio of the difference between the middle-block current I_1 and the lower-block current I_2, i.e., the 'not'-recycled current ratio ($1-I_2/I_1$), was observed with monitor pins.

Figure 6(a) shows the fluctuation for the two types of proposed dividers and the conventional capacitance type. For the MOS-diode type, the maximum current ratio has to be under 20% to suppress the fluctuation of V_{int} to 0.1 V. For the comparator type, the fluctuation is kept at 0.1 V independently of the current ratio I_1/I_2. The power consumption for the circuits managing one intermediate voltage is 6 mW. In the case of 100 mA current supply, the efficiency of this architecture is 98%, which is a 5% improvement compared with down converters.

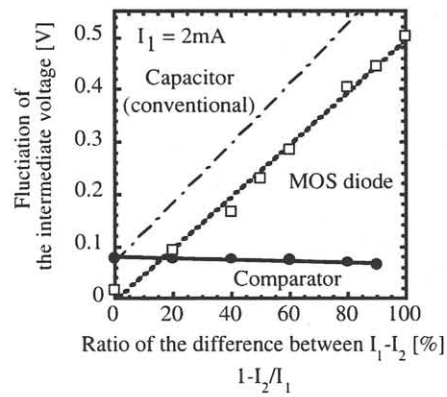

Fig. 6. Comparison of the fluctuation versus the current ratio for the two dividers.

5. Summary

The proposed Stacked-CMOS architecture reduces the power consumption of LSIs by the square of the number of divisions and the amount of current by the number of divisions. A new voltage divider circuit provides voltage stability of 10% within 6 mW excess power consumption.

References

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(3) H. Yamauchi et al., 94 VLSI Circuits Digest of Technical Papers. pp. 21-22, 1994.