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A Dynamically Reconfigurable Processor with Multi-Mode Operation Based on Newly Developed Full-Adder/D-Flip-Flop Merged Module (FDMM)

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1. Introduction

Dynamically customizable and reconfigurable hardware architecture for a specific task on demand is one of the most important issues to bring out a novel-computing paradigm in the era of system LSI. This is because it can fill a wide gap between hardware performance and software programmability [1]. The gap has been shown, for instance, as a difference between application-specific LSI (ASIC) with intensive performance and field programmable gate array (FPGA) with intensive programmability. Moreover, in conventional FPGA, customizable modules are composed of large combinational logic part and optional flip-flop part to perform any functions by utilizing its vast programmability. Therefore, developing an original type of customizable module that has both ASIC's and FPGA's merit, which eliminates redundant programmability preserving necessary specific functionalities for performance, is most promising in order to realize dynamically reconfigurable processor. This is our focus.

We have developed an original full-adder / D-flip-flop merged module (FDMM) and fabricated a chip including a 4 x 4 array of FDMMs with $0.6\mu m$ CMOS technology[†]. Utilizing the chip and circuitry concept, near to the future, we are planning to apply these to some signal processing applications such as encrypting, image filtering, multi-task digital signal processing, and customizable-coding of microprocessor, memory, and other standard products.

In this paper, we propose the developed FDMM and introduce the fabricated system architecture of dynamically reconfigurable multi-mode processor based on FDMM in detail.

2. Full-Adder / D-Flip-Flop Merged Module (FDMM)

A schematic and operation of FDMM are shown in Fig. 1. This module is composed of main functional block (shaded) and sub-control circuit. This module can be operated in multi-mode. When a control signal "sel" = 1, the module acts as a full-adder circuit (Logic MODE); and when "sel" = 0, it acts as a D-flip-flop circuit (Flip-flop MODE). Note that FDMM has an ability to perform both logic and flip-flop functions with a small transistor counts by merging common part of full-adder and D-flip-flop circuit in contrast with traditional logic modules in FPGAs, these are preparing *both logic and flip-flop* inside. It is a characteristic feature of this study.

From the viewpoint of logic functionality, full-adder can realize sufficient logic functions such as 3-XOR, 3-Majority, 2-AND, 2-OR, 2-XOR, 2-XNOR, etc. It is very suitable essentially for arithmetic operation based on AND/OR signal processing that is frequently used in many specific compute-intensive applications besides.

3. Dynamically Reconfiguration Method

To reconfigure the hardware dynamically, we have constructed our system utilizing multi-context architecture [1-2], and developed a context memory block (CMB) to fit our concept. It reconfigures the FDMMs and routing states among them shown as Fig. 2. Context is selected by a context number, and read out into control signal "sel" of FDMM and into a interconnection switches. Since the system-reconfiguration is achieved only by changing the context number, reconfiguration time is the order of nanoseconds. In other words, it enables us to reconfigure the hardware dynamically.

Another feature of this CMB is a self-arbitration. We designed it for a word-line to be given a write-access automatically to an unselected memory. Therefore, there is no need to manage a conflict, though the CMB is dual-port; and we can write in anytime with no affection onto a selected one to read.

4. Dynamically Reconfigurable Multi-Mode Processor

Integrating FDMM and CMB, we have fabricated a test chip of dynamically reconfigurable processor with multi-mode operation. This chip contains an array of 4 x 4 FDMMs and they can be routed by the interconnect switches. Each of FDMMs and interconnect switches has one 2-bit-CMB, therefore, this chip has a capacity to reconfigure two pages of programs. As shown in Fig. 3, we prepared two types of routing resources, i.e., local and global lines. The former is a routing for fast signal propagation onto the neighboring 3 modules at the lower stream, and the latter is one for feeding signals up and down to the stream into any horizontal and vertical directions.

Figure 4 is a layout of this chip. It is fabricated with $0.6\mu m$ CMOS technology. The chip size is $4.5mm \times 4.5mm$ sq, and the area of one FDMM is 49 x 136 μm^2 . Most of the processor's area is occupied by many CMBs for an evaluation, but there are also many redundant CMBs in an actual usages, therefore further compact design is possible. Now we have been attempting several solutions to reduce these CMBs and enhance the FDMM's integrity onto the next chip design, the results may be reported as the occasion serves.

[†] This chip is under fabricating now but scheduled to be fabricated and delivered until the conference will be held. (Delivering date: 17 Apr. 2000)

Figure 5 is a post-layout simulation result of FDMM to confirm its operation. When control signal "sel" = 0, input "A" appears at output "X" with a delay in synchronizing to clock signal. And when "sel" = 1, "X" and "Y" outputs XOR and Majority of three input "A", "B", and "C" respectively.

It has made sure that FDMM behaves answering our aim.

5. Conclusion

We have developed and proposed FDMM featuring multi-mode operation in order to realize dynamically reconfigurable processor, which is the most promising candidate to bring out a novel-computing paradigm. In order to improve the potential of FDMM, we have fabricated a proof-of-concept test-chip by integrating FDMM and CMB, which enables



Fig. 1 A schematic of developed full-adder / D-flip-flop merged module (FDMM) featuring multi-mode operation



Fig. 2 A circuit diagram and its operation of 2-bit dual-port context memory block (CMB) with self-arbitration mechanism

hardware to reconfigure dynamically. Since the base concept of FDMM is unique, we hope that FDMM exploits some advanced signal processing applications and may fill a gap between hardware performance and software programmability to jump the present computing into a novel one.

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Fig. 5 Post-layout simulated transient behavior of FDMM



Fig. 4 Chip layout of dynamically reconfigurable processor with multi-mode operation based on FDMM and CMB