Extended Abstracts of the 2000 International Conference on Solid State Devices and Materials, Sendai, 2000, pp. 378-379

E-5-4

# A 3.26 $\mu m^2$ Full CMOS SRAM Cell Using Non-Overlap Contacts for Super Low Power Applications

H.S. Ha, J.E. Song, H.S. Chang, K.H. Lee, S.G. Kim, K.J. Kim, and K.T. Kim
SRAM Team, Samsung Electronics Co., Ltd.
San#24, Nongseo-Ri, Kiheung-Eup, Yongin-City, Kyungki-Do, Korea(ROK)
Phone:+82-331-209-6177 FAX:+82-331-209-5624 E-mail:turbo11@samsung.co.kr

## ABSTRACT

A 3.26$\mu m^2$ 6T full CMOS SRAM Cell has been developed using the non-overlap contact process with design rule of 0.18$\mu m$. The high-leakage probability of non-overlap contacts was suppressed by making SiN spacer on the edge of active. It could protect the boundary area between active and field from over-etching for forming contacts. We have obtained good characteristics of the buried-channel PMOSFET with Lg=0.20$\mu m$ as the load device in the cell which show stable operation at the low voltage under 0.5V. A 8Mb low power SRAM with small size and low cost was successfully integrated with low standby current below 4uA at high temperature(85℃).

## INTRODUCTION

According to rapid development of hand held machines, there is a strong demand on SRAM of very low standby current and higher packing density. The non-overlap contact process is effective to reducing cell size without advanced lithography technology, but has been known to have the high leakage current characteristics because of active recess occured in the step of contact etch and to be inadequate for low power applications. SiN Guard-Ring(SiN Visor) on the upper edge of active was reported to improve the transistor characteristics induced by steep sidewall of STI[1] and to making landing-pad of contacts without etch stopper in salicide process[2] which is not preferable to low power device because of its high junction leakage. Therefore, in this study we improved the leakage of non-overlap contact using both SiN visor and etch stopper for low leakage current. The buried-channel(BC)-PMOSFET employing n+poly Si gate has many advantages such as low process costs, no boron penetration and no poly Si depletion, but as gate length is shorter, we have had a difficulty in the use of BC-PMOSFET owing to its Short-Channel Effect(SCE) and Punchthrough[3]. However in this study we integrated and optimized BC-PMOSFET, which had stable characteristics at small gate length of 0.20$\mu m$.

## PROCESS INTEGRATION

Fig.1 shows the layout of (a) SRAM cell and (b) top view after the step of W-plug contact and L.I. (Local-Interconnect) damascene etch. The small cell size of 3.26$\mu m^2$ could be achived by adopting non-overlap contact. The only 60nm overlap enlarges 12.1%(3.72$\mu m^2$). Fig.2 shows the cross-sectional SEM pictures of cell. Table.1 indicates the fabrication process flow of 8Mb low power SRAM. STI had depth of 0.35$\mu m$ and gapfilled with HDP(High Density Plasma) Oxide and planarized with CMP. Retrograded twin well were used for 0.24$\mu m$ space in N+/N+ and P+/P+, 0.44$\mu m$ space in N+/P+ isolations. 5nm nitrided oxide was grown as gate oxide. W-polycide was used as gate material and the minimum size of the gate length was 0.20$\mu m$ in NMOSFET and PMOSFET. By using the step between field oxide and Active, SiN visor could be formed on the edge of active at the process of the gate spacer etch back. Contact etch stopper of SiN film is deposited and followed by ILD layer formed and planarized. The non-overlap contact of the bottom size of 0.18$\mu m$ was etched with selectivity between ILD and SiN. An aspect ratio of this small deep contact was about 4. This high aspect ratio contact hole was filled with Ti/ TiN barrier metal and W using CVD method. W lines with 0.36$\mu m$ pitch were made up using damascene process for L.I. and Vdd/Vss lines in a cell. The cell had one-Al-metal layer which was used for bit lines.

## NON-OVERLAP CONTACT AND LEAKAGE

Fig.3 shows vertical view of SiN visor and SiN etch stopper on the edge of active before and after formed contact. SiN etch stopper and visor protected the field area from being etched during contact etching process through ILD and there is no recessed etch at the contact edge on field as shown in Fig.3(b)(d). Fig.3(e) shows that the leakage current of non-overlap contact is not different from overlap things. The dependance of contact resistance on overlap size could be explained by the touch area between contact metal and active. Fig.4 also shows that SiN visor with etch stopper is more effective than that without etch stopper for control leakage current. The leakage current level of non-overlap contact with SiN visor and etch stopper has no difference to that of sufficiently overlapped contact. The standby current characteristics of fabricated 8Mb SRAM was good as below 0.4$\mu A$/Mb and there is no difference between products with 60nm overlap and without overlap as shown in Fig.5.

## ELECTRICAL CHARACTERISTICS

Data described in this paper were measured at 85℃. Fig.6 shows the Vth and BV depentance on gate length and stable characteristics to 0.20$\mu m$. SCE of BC-PMOSFET could be improved by adopting single drain structure. Isolation characteristics and the typical transistor Vg-Id curves are shown in Fig.7 and Fig.8, respectively. DC measurement results are also summarized in Table.2. The cell was stably operated down to a supply voltage of 0.5V as shown in Fig.9. The standby current of 8Mb SRAM was 4$\mu A$. The address access time(taa) of 8Mb SRAM was 60ns at 2.0V and it functioned well down to Vdd=1.3V as shown in Fig.10.

## CONCLUSION

The SiN visor and etch stopper on the edge of active are effective to obtain low leakage current characteristics of non-overlap contact and we could reduce more than 12% of cell size by using this skill in 0.18$\mu m$ design rule for very low power SRAM. Buried-Channel PMOSFET with the 0.20$\mu m$ of gate length was realized in the 3.26$\mu m^2$ cell of 8Mb SRAM, which show stable operation at as low as 0.5V. 8Mb low-power SRAM was integrated successfully with low standby current.

## REFERENCES

[1] T. Ogura, et al., Sympo. on VLSI Tech. 210 (1998)
[2] K. Noda, et al., IEDM Tech. Dig., 847 (1997)
[3] T.Tanaka, et al, Sympo. on VLSI Tech. 109 (1999)

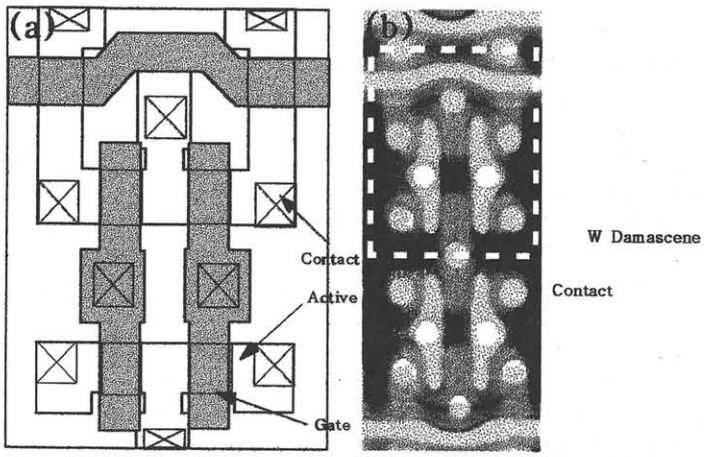



**Fig.1** (a)Layout and (b)Top View of SRAM Cell(1.6um×2.04um) with Non-overlap Contact

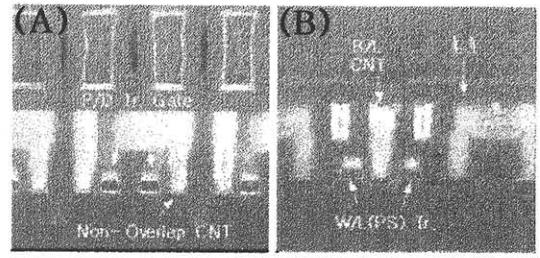


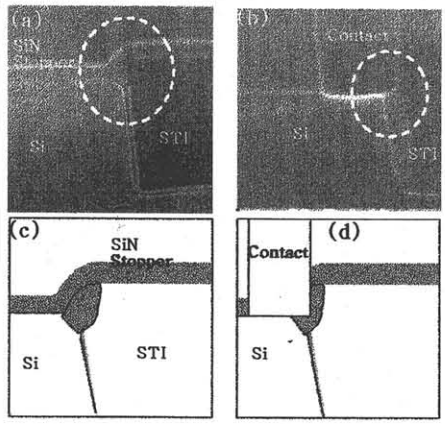

**Fig.2** Cross-sectional SEM of Non-overlap Contact Cell (A) X-direction (B) Y-direction

| | Vth (V) | Idsat(μA/μm) @Vd= Vg= 2.0V | Idoff(/μm) @Vd= 2.0V | BV(V) @10nA |
|---|---|---|---|---|
| NMOS | 0.80 | 230 | ≤ 10 fA | ≥ 6 V |
| PMOS | 0.78 | 150 | ≤ 10 fA | ≥ 6 V |

**Table.2** Device Parameter of 8M bit low-power SRAM(50Å Gox, @85℃)

- Trench Isolation
- STI Gap Fill (HDP)
- Retrograde twin Well
- Gate Patterning
- LDD Formation (N-LDD,P-LDD)
- Spacer Formation & S/D Implantation
- S/D Anneal
- ILD-1 Deposition & Planarization
- W Plug Contact Formation
- Damascene Local Interconnection
- Metal Formation(Cell:1-Metal)

**Table.1** Fabrication Process Flow



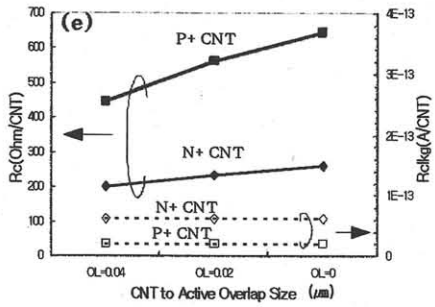




**Fig.3** Schematics of Non-overlap Contact and Contact Resistance, Leakage Current (@2.6V) according to CNT Overlap Size(85℃)

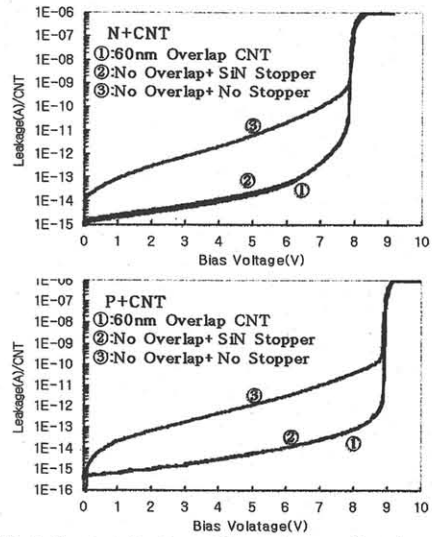



**Fig.4** Contact Leakage Current according to Contact Overlap Size & SiN Stop-Layer (@2.6V,85℃)

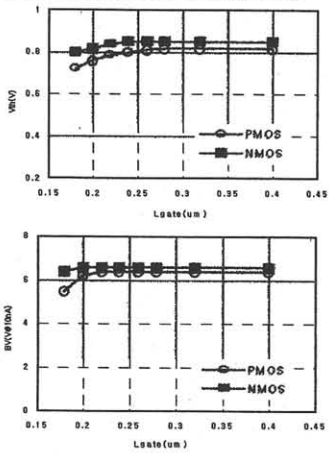



**Fig.6** Vth roll-off and Tr BV Characteristics (85℃)

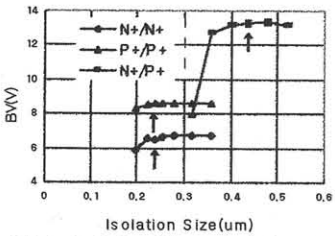



**Fig.7** Isolation Characteristics (85℃)

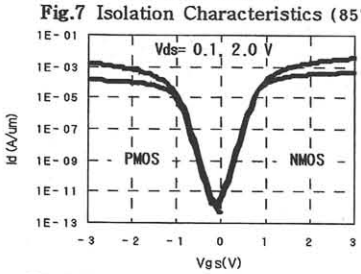



**Fig.8** Vg-Id and Characteristics of NMOS and PMOS FET (85℃)

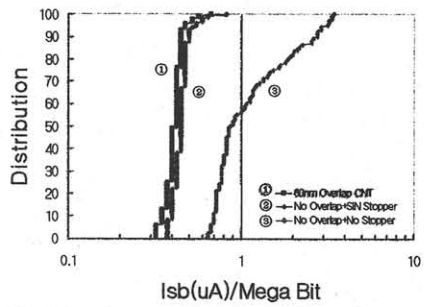



**Fig.5** Isb Characteristics of 8M bit SRAM (85℃)

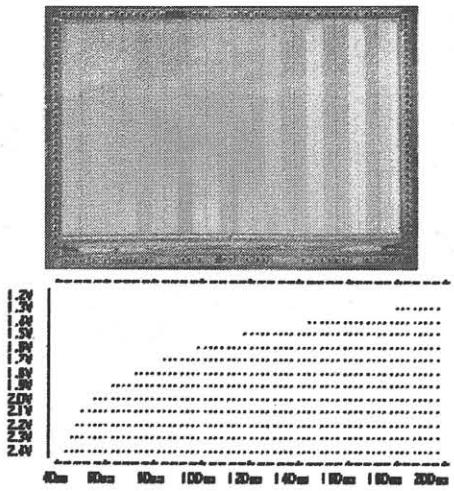


**Fig.10** Microphotograph of 8M bit SRAM (7952μm×5200μm) and Taa Plot(85℃)

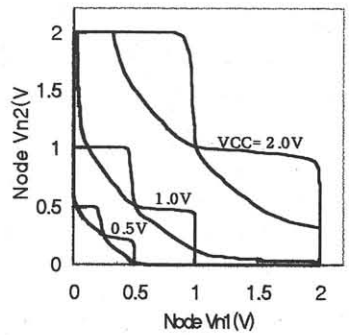



**Fig.9** DC Characteristics of SRAM Cell (85℃)