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Three-Dimensional Capacitance Analysis in an SRAM Cell

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1. Introduction

As the packing density in ULSIs increases, the interconnect delay becomes a serious problem in achieving high-speed operation. Thus, we need to accurately estimate the interconnect capacitance and design a 3-dimensional (3D) layout to minimize the interconnect capacitance.

However, 3D analysis requires long CPU time and large memory area. Therefore, in an effort to reduce the design period of ULSIs, 2D analysis has been performed for the main cross sections of the whole interconnect structure. But this analysis includes error because it does not take into account the 3D effects [1] inherent in a real structure. And this type of analysis cannot be applied for some complex structures.

Thus, we analyzed the whole 3D interconnect capacitance in an SRAM cell. Our analysis used Green's function method, which does not require large computational resources. Three-dimensional effects are included in the whole-structure calculation, and all capacitances among conductors can be obtained simultaneously. In this paper, we will report novel 3D effects and examine them in detail.

2. Method of Calculation

The calculations by the Green's function method were performed using the TRISIM1 [2] program to analyze the electrostatic field. This method requires a smaller memory area than other methods [1], because calculation meshes are defined only on the surface of conductors, not all over the 3D space containing the interconnect. And coupling capacitances among all conductors can be obtained simultaneously.

3. Interconnect Structure in an SRAM Cell

The whole interconnect structure in an SRAM cell was analyzed. The cell had three interconnect layers (from M0 to M2), and five parallel lines were located at M2. The line S4 was located at layer M1, and crossed under the lines at M2 (Fig. 1). All these lines connect to the Si substrate through vertical vias and horizontal lines.

4. Three-dimensional Capacitance Analysis

We calculated N(N-1)/2 coupling capacitances in a cell that consisted of N conductors. The significant results were as follows. (1) The overall S1-S2 capacitance was 15% larger than the S1-S3 capacitance, although S2 and S3 were symmetrical with respect to S1. The capacitance difference occurred because the short via connected to S2 was adjacent to S1 (as indicated by arrows in Fig. 2), while the via connected to S3 was not adjacent to S1. (2) The S1-S4 capacitance (shown as inset (a) in Fig. 3) consisted of three components ((b)-(d)), and the main contribution was short line parallel to S4 (d), not long line or via that crosses over S4 ((b) and (c)). (3) The capacitance between a contact via (named CNT) and a MOS gate was comparable to the overall S1-S2 and S1-S3 capacitances.

To examine the 3D effects in (1)-(3) in detail, we decomposed the interconnect structure and ran more calculations for the important parts.

(1) capacitance of parallel lines with vias

To examine the via connection strength, we calculated the capacitance between conductor lines for three cases : (a) parallel lines without a via connection, (b) a via connected beneath the adjacent line, (c) vias connected on and beneath the adjacent line (Fig. 4). In the figure, the capacitances are normalized by a parallel plane capacitance in inset (a) (C_f). In all cases, the normalized capacitance increased as the distance between the lines increased. The normalized capacitance for via-connected lines ((b) and (c) in Fig. 4) was larger than that for parallel lines (a). When the distance between the lines was one to three times longer than the line width, the capacitance for (c) was always 1.2-1.5 times larger than that for (a). This indicates that the electric field terminated by surface of vias increases the capacitance.

(2) capacitance of parallel lines

We calculated the capacitance between two parallel lines. The length of one line was fixed at 50 μm, and that of the other line was variable and shorter than 50 μm. In Fig. 5, capacitance between the lines is normalized by parallel plane capacitances (C_v), where $C_v = \varepsilon tr / d$. The normalized capacitance increased as the line length r decreased (Fig. 5 (a)), and the capacitance increased as the distance between the lines, d, increased (b). This indicates that when the shorter line length r decreases, the electric field terminated by the parallel plane of the area tr shrinks, and as a result, the fringing field terminated by the side walls expanses relatively. When the line width w was equal to r and d, the normalized capacitance was about 8.

(3) capacitance between CNT and gate

To examine the capacitance between vertical and horizontal conductors, we calculated capacitances when a gate approached the middle point of two CNTs. As shown in Fig. 6 (a), as the gate approached the middle point, the CNT-CNT capacitance decreased while the CNT-gate capacitance increased. The CNT-gate capacitance reached a maximum when the gate reached the middle point of the CNTs.

Furthermore, we estimated the influence of the top and bottom of the conductors on capacitance. The maximum of the CNT-gate capacitance saturated as h / t increased to infinity (Fig. 6 (b)). Considering the curves here to be parallel to each other, we obtained the zero-thickness capacitance of 9×10^{-18} F (Fig. 6 (c)). This value is the capacitance contribution from both top and bottom of the CNTs and the gate when the gate height is infinity.

These results indicate that the CNT-gate distance should be as large as possible to minimize capacitance.

5. Conclusion

We analyzed the 3D capacitance for the whole interconnect structure in an SRAM cell and found novel 3D effects. Detailed examination of these effects showed that our analysis method is useful in designing high-speed ULSIs.

Acknowledgment

We would like to thank Dr. N. Kobayashi of Hitachi's Device Development Center and Dr. K. Ishibashi of Hitachi's Central Research Laboratory for their fruitful discussions.

References

[1] P. E. Cottrell et al., *IEDM'82* p548 (1982)
[2] R. Kamikawai et al., *Proc. of the IEEE Int'l Conf. on Computer Design : VLSI in Computers & Processors*, p434, The Computer Society of the IEEE, DC, USA (1987)

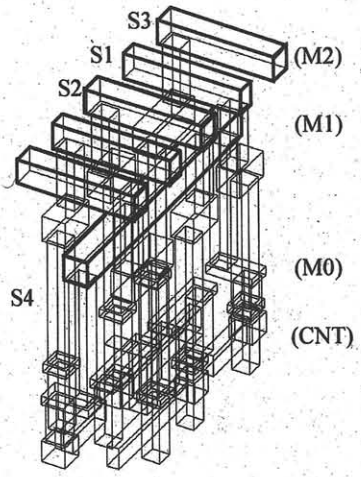


Fig. 1 Interconnect structure in an SRAM cell.

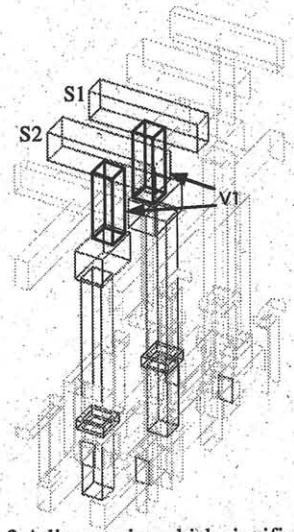


Fig. 2 Adjacent vias which significantly affect overall S1-S2 capacitance.

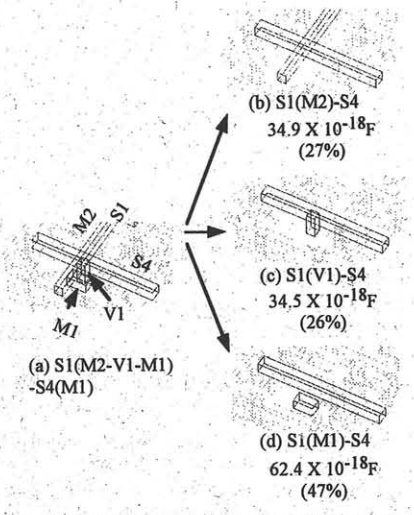
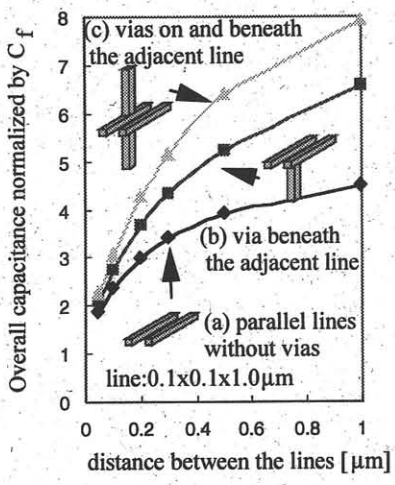
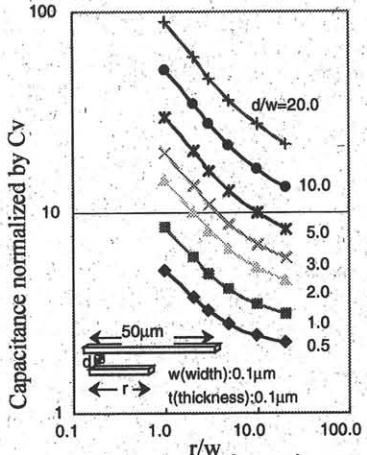
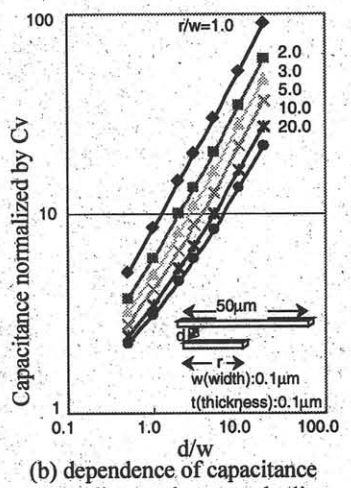


Fig. 3 Partial capacitance contribution to overall S1-S4 capacitance.





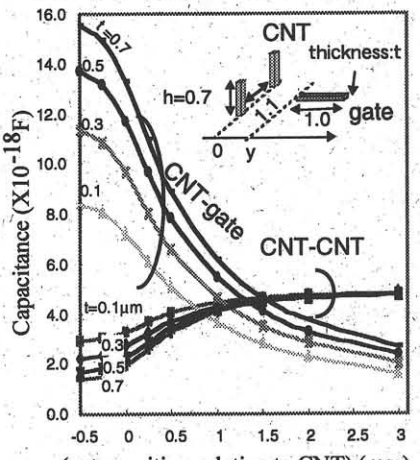
(a) dependence of capacitance on line length



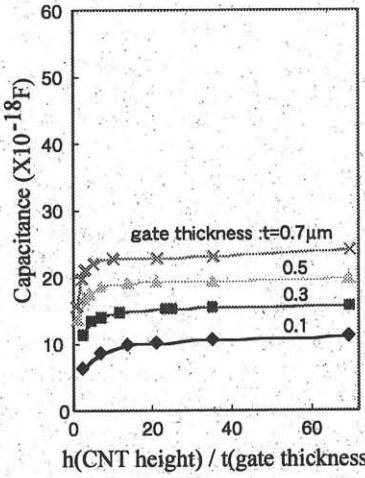
(b) dependence of capacitance on distance between the lines

Fig. 4 Effect of via connected to adjacent line to overall capacitance (Cf: parallel plane capacitance in (a))

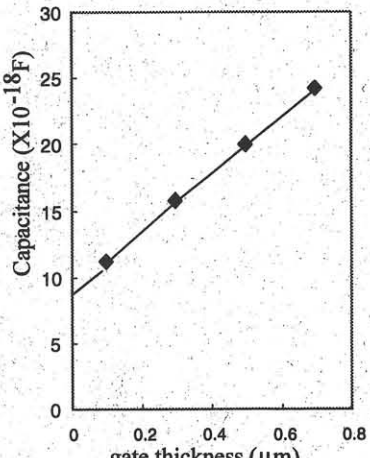
Fig. 5 Fringing effect on overall capacitance between parallel lines. (Cv : parallel plane capacitance, where Cv = εtr / d)



(a) dependence of CNT-gate and CNT-CNT capacitance on gate position relative to CNT.



(b) dependence of CNT-gate maximum capacitance (when y= -0.5 μm in (a)) on CNT height / gate thickness.



(c) dependence of CNT-gate maximum capacitance (when h / t =70 in (b)) on gate thickness.

Fig. 6 CNT-gate and CNT-CNT capacitance