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# Low-Power Area-Efficient Design of Parallel Pipeline A/D Converters

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## 1 Introduction

A/D converters are the essential analog macrocells in mixed analog-digital system LSI's. The power dissipation and the silicon area occupation of the logic circuits can be directly reduced by the process technology scaling. However, for analog circuits, the technology scaling does not always lead to a great reduction of the power and the area. Therefore, low-power and area-efficient design method of embedded A/D converters becomes important to achieve totally high cost performance. In this paper, we propose a design method of embedded A/D converters in mixed-signal system LSI's using 1.5bit/stage interleaved pipeline architecture and a low-power regulated cascode amplifier. We point out that the interleaved pipeline scheme in very effective for low-power design of high-speed A/D converters. The estimated power dissipation of the designed 10bit high-speed A/D converters is extremely low compared with those previously reported.

## 2 Architecture

The high-speed A/D converter(ADC) architecture employed here is a 1.5 bit/stage parallel pipeline ADC. The functional block diagram is shown in Fig. 1. It consists of a time-interleaved array of pipeline ADC's and each channel consists of an input track-and-hold(T/H) stage followed by a cascade of 1.5bit/stage pipeline stage. The pipeline ADC stage consists of a multiply-by-2 residue amplifier shown in Fig. 2(a) and two comparators and control logic circuits. A low-power amplifier with less DC bias current using dynamic biased regulated cascode configuration shown in Fig. 2(b) is used for the ADC stage [1].

In the amplifier design, there are 4 design parameters in each transistor; effective gate bias ($\Delta V = V_{GS} - V_T$),channel length ($L$), channel width ($W$) and bias current ($I_0$). The effective bias voltage is closely related to the output voltage swing of the amplifier, and is determined from the specification of the power supply and the output voltage swing. The channel length of each transistor is chosen as the minimum to meet the condition of the required open loop gain. In each transistor, the ratio $I_0/W$ is given by

$$\frac{I_0}{W} = \frac{\mu_{eff} C_{ox} \Delta V^2}{2L}. \quad (1)$$

Since $\Delta V$ and $L$ are fixed first, the ratio $I_0/W$ must be unchanged during the design procedure of $W$ or $I_0$. The bias current $I_0$ is determined to meet the settling time requirement under the given sampling frequency. Parameters of each transistor is designed as shown in Table 1. Three essential design parameters of $\Delta V_0$, $L_0$ and $W_0$ are determined by the ADC specification. Either $W_0$ or $I_0$ is determined, the other is determined automatically by Eq. (1). The settling time of each pipeline ADC stage is calculated as

$$t_s = C_A \frac{V_{ref}}{I_o} + \tau \left( \ln \left( \frac{2C_s + C_i}{C_s} \frac{1}{e_{st}} \frac{I_0/g_m}{V_{ref}} \right) - 1 \right) \quad (2)$$

where

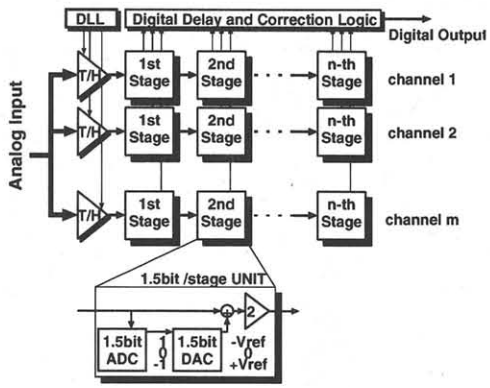


**Fig. 1** 1.5bit/stage parallel pipeline A/D converter.

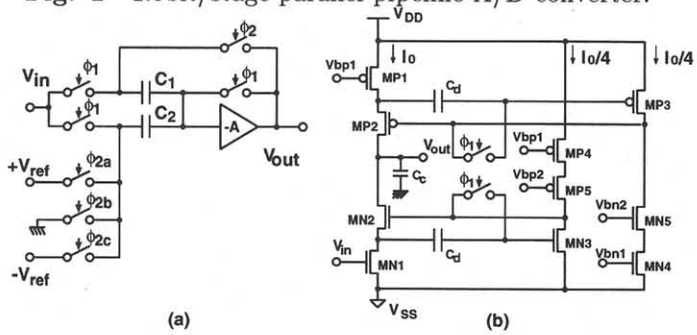


**Fig. 2** (a)Multiply-by-2 residue amplifier and (b)High gain cascode amplifier using dynamic biased regulated cascode technique.

$$\tau = \alpha \left( 5C_s + 3C_i + 2(C_o + C_c) + \frac{C_i}{C_s}(C_c + C_o) \right) \frac{1}{g_m}, \quad (3)$$

$$C_A = 7C_s + 3(C_s + C_c) + \frac{C_s^2}{2C_s + C_i}, \quad (4)$$

where $e_{st}$ is the settling error, $C_s$ is the capacitance of $C_1$ and $C_2$ in Fig. 2(a), $C_o$ and $C_i$ are the output and input parasitic capacitances of the amplifier, respectively, and $C_c$ is the compensation capacitance at the output and $\alpha$ is a constant to take into account the resistive component of load circuits and is determined by the comparison with the SPICE simulation of actual circuits.

## 3 Design Example

High speed parallel pipeline ADC's with four sampling frequencies specified in Table 2 are designed here. The technology assumed is $0.6\mu m$ double polysilicon CMOS. The number of pipeline stages is 12 for 10bit resolution to use digital domain error correction. The unit capacitance $C_s = 0.4$pF is chosen here to obtain the SNR of 61dB. The unit effective gate bias voltage $\Delta V_0$ is calculated to be $0.19V$ from $V_{supply} = 2.5V$, $V_s = 1.5V$ and Table 1. For

**Table 1** Parameters of each transistor ($a = \mu_{eff}n/\mu_{eff}p$).

| Transistor | $L$ | $W$ | $\Delta V$ |
|---|---|---|---|
| $MP1$ | $2L_0$ | $2W_0$ | $\sqrt{a}\Delta V_0$ |
| $MP2$ | $L_0$ | $2W_0$ | $\sqrt{a/2}\Delta V_0$ |
| $MP3$ | $L_0$ | $W_0/2.9$ | $2\sqrt{a}\Delta V_0$ |
| $MP4$ | $2L_0$ | $W_0/2$ | $\sqrt{a}\Delta V_0$ |
| $MP5$ | $L_0$ | $W_0/2$ | $\sqrt{a/2}\Delta V_0$ |
| $MN1$ | $L_0$ | $W_0$ | $\Delta V_0$ |
| $MN2$ | $L_0$ | $W_0$ | $\Delta V_0$ |
| $MN3$ | $L_0$ | $W_0/16$ | $2\Delta V_0$ |
| $MN4$ | $L_0$ | $W_0/4$ | $\Delta V_0$ |
| $MN5$ | $L_0$ | $W_0/4$ | $\Delta V_0$ |

**Table 2** Examples of specification.

| Parameter | Value |
|---|---|
| Technology | $0.6\mu m$ CMOS |
| Resolution | 10bit |
| Sampling frequency | (a)20MHz (b)50MHz (c) 80MHz (d) 150MHz |
| Supply voltage | 2.5V |
| Full scale | 1.5V |
| SNR | 61dB |
| INL | $\langle$ 0.5LSB |

**Table 3** Summary of estimation.

| $F_s[Hz]$ | $M$ | $I_0$ $[\mu A]$ | $W_0$ $[\mu m]$ | Power$[mW]$ | Area $[mm^2]$ |
|---|---|---|---|---|---|
| 20M | 1 | 143 | 103 | 6.4 | 0.91 |
| 50M | 4 | 64 | 46 | 11.5 | 3.48 |
| 80M | 4 | 143 | 103 | 25.8 | 3.62 |
| 150M | 8 | 126 | 91 | 45.6 | 7.21 |

10bit resolution and INL $\langle$ 0.5LSB, the settling error of less than 0.1% and open-loop gain of 70[dB] are required. $L_0 = 1.2\mu m$ is chosen because the resulting open-loop gain is 80dB with sufficient margin of 10dB. Figure 3 shows SPICE simulation results of the settling time for $e_{st} = 0.1\%$ in the multiply-by-2 residue amplifier as a function of $I_0$. The solid line in Fig. 3 is that of analytical model in the case of $\alpha = 2$ in Eq. (3). The analytical model with $\alpha = 2$ is agree with the simulation result.

Using the analytical model of the settling time given by Eq. (2), the relationship between the normalized power dissipation and the sampling frequency is plotted as shown in Fig. 4 for the number of ADC channels of 1, 2, 4, 8 and 16. This result means that parallel pipeline ADC architecture is useful to reduce the power dissipation especially for high sampling frequency.

Although the increase in the number of ADC channels leads to the reduction of power dissipation, the reduction is limited to the normalized power of 1, and the total ADC area is increased. For low-power area-efficient design, we need a cost function given by the product of power and area. Figure 5 is the normalized cost function as a function of the sampling frequency. From Fig. 5, the optimal combination of the power, the area and the number of ADC channels can be estimated under the given sampling frequency. The summary of the estimation is shown Table 3. Although only the static power is estimated, the power dissipation is very low compared with 10bit high-speed A/D converters previously reported .

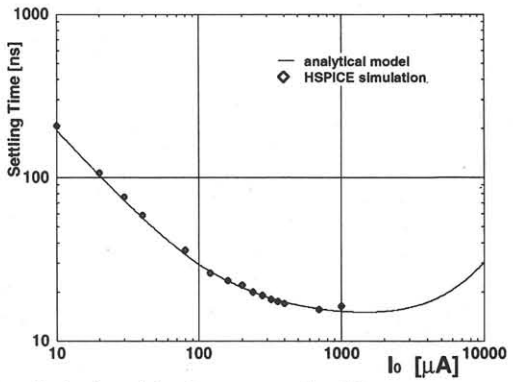


**Fig. 3** Relationship between the bias current and settling time.

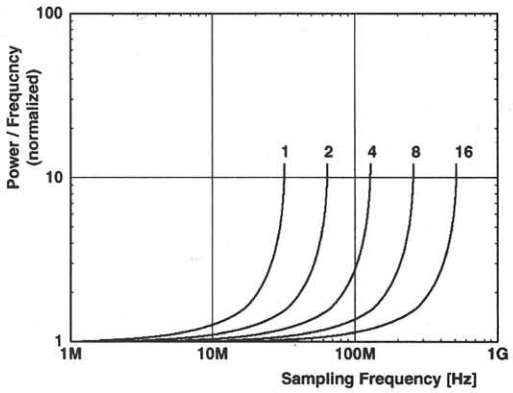


**Fig. 4** Normalized power versus frequency.

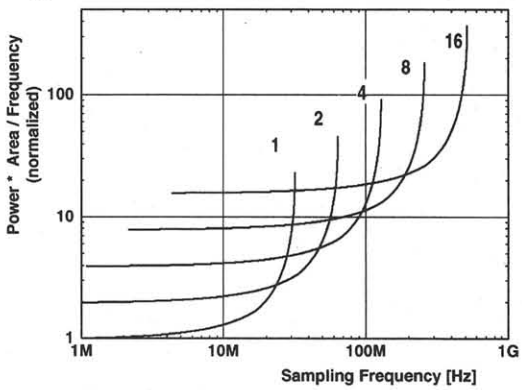


**Fig. 5** Cost function versus sampling frequency.

## 4 Summary

In this paper, a low-power area-efficient design method for high-speed embedded A/D converters has been described. A 1.5bit/stage time-interleaved pipeline architecture with a dynamic biased regulated cascode amplifier is useful for low-power A/D converter IP which can be adapted to a wide range of specifications of conversion frequency and resolution.

**Acknowledgement**

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## References

[1] D. Miyazaki, S. Kawahito and Y. Tadokoro "Low-Power Area Efficient Pipelined A/D converter Design Using Single-Ended Amplifier," IEICE trans. fundamentals, vol.E82-A, no.2, pp.293-300, Feb. 1999.