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Novel FFT LSI for OFDM Using Current Mode Circuit

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1. Introduction

Orthogonal frequency division multiplexing (OFDM) is available for indoor/outdoor wireless local area network (LAN) and wireless local loop (WLL). Conventionally, the fast Fourier transform (FFT) LSI that is the main signal processing of OFDM is implemented using digital signal processing (DSP). However, in high operating speed, the large power consumption is generally needed using DSP. We have already proposed current-cut switched current matched filter (CC-SIMF) with power consumption less than 10mW[1]. Implementation of SIMF LSI using 0.8μm digital compatible process is reported[2] and measured operation frequency is up to 20MHz [3]. SI circuit with current-cut is promising for low power analog signal processing.

In this paper, we present a novel design method of low power FFT LSI for OFDM using the current mode circuit.

2. New design method of FFT LSI for OFDM.

Typical OFDM spectrum is shown in Fig.1. OFDM signal for digital communication consists of a large number of orthogonal sub-carriers. For example, in IEEE802.11a, 48 sub-carriers with the bandwidth of 20MHz is required, so that 64-point at the clock rate of 20MHz is required for FFT [4]. The orthogonal sub-carriers can be generated using the discrete Fourier transform (DFT) algorithm. Figure 2(a) shows a typical DFT matrix. Generally, FFT algorithm is used for high speedy computation of DFT matrix. Figure 2(b) shows the 8x8 DFT matrix. The 8x8 DFT matrix can be converted to complex and integer matrix as shown in Fig. 2(c), which is called FFT matrixes in this paper. Each component of complex matrix of FFT matrixes can be described as $a+jb$, where a and b ($-1 \le a, b \le 1$) is the real number.

We propose the simplification method using rounding for the component of FFT matrixes. Rounding means, for example, that the number 0.707+j0.7071 is rounded to 0.7+j0.7 as shown in Fig. 2(d). The complex matrix after the rounding is called as rounded matrix of FFT matrixes. Figure 3 shows the bit error rate (BER) using rounding. The rounding step "0.2" means a and b are rounded each 0.2. BER using FFT matrixes with rounding step of 0.2 has little difference from BER using ideal FFT. The simple circuit structure of FFT LSI for OFDM could be designed by rounding the components of FFT matrixes.

3. Implementation of FFT LSI for OFDM

Figure 4 shows schematic of FFT matrixes. The accumulation block corresponds to integer matrix of FFT matrixes and the weighted block corresponds to rounding matrix. The summation can be realized wired-or current summation. Weighted coefficient is decided from component of rounded matrix. The weighted operation can be carried out using gate-width ratioed current mirror circuit. Figure 5 shows the gate-width ratioed current mirror circuit. Gate widths of W1 and W2 are determined by the weighted coefficient. For example, when the weighted coefficient is 0.7, gate-width ratio is W1/W2=10/7. In this case, current signal is reduced to 0.7.

Figure 6 shows the conventional current delay flip flop (C-DFF). The C-DFFs memorize serial input current data. The C-DFF is constructed with three current memory (CM) cells. The CM cell in Fig. 6 has the components of current source, sample switches and a CM MOSFET [3]. Input current is memorized at the gate voltage of CM MOSFET and transferred to another CM by switching of sample and hold. Dummy MOSFET for reduction of current error of basic cell is used [5]. Figure 7 shows the layout of designed 8-point FFT LSI using 0.8 μm CMOS Technology.

Power consumption of 64-point FFT LSI for OFDM is estimated. Using DSP, the power consumption is generally needed more than 100mW[6]. The power consumption of SIMF using current-cut is 19.7mW. The power consumption is independent of operating frequencies. SI FFT has a potential of operating frequency of over 100MHz at the same power consumption, because the sampling period of CM is less than 5nsec[3]

4. Conclusion

We have proposed novel FFT LSI for OFDM using current mode circuits. Rounding the component of FFT matrixes leads the easy implementation of SI circuits. The 8-point FFT LSI has been designed and implemented using 0.8μm CMOS technology. Estimated power consumption of 64-point FFT LSI using current mode circuits is less than 19.71mW. Low power FFT LSI using current mode has great advantage for mobile terminals of wireless LAN and WLL.

References

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[4] IEEE802.11a.
[5] Minkyu Song, Yongman Lee, Wonchan Kim. IEEE Solid State Circuits: VOL.28, No.2, 1993.
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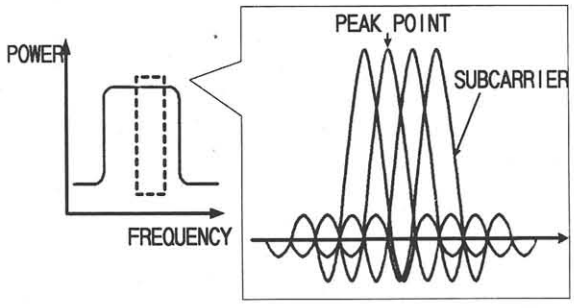

Fig.1 Typical OFDM spectrum with sub-carriers.

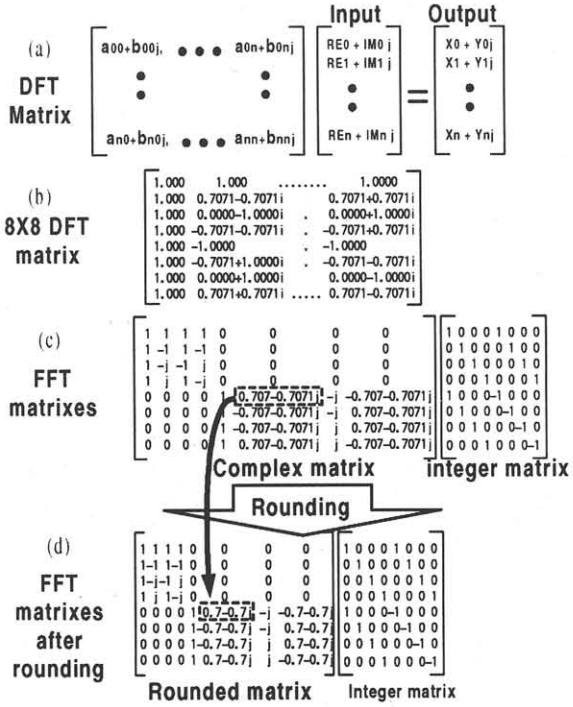

Fig.2 The matrix calculation flow revised with FFT algorithm.

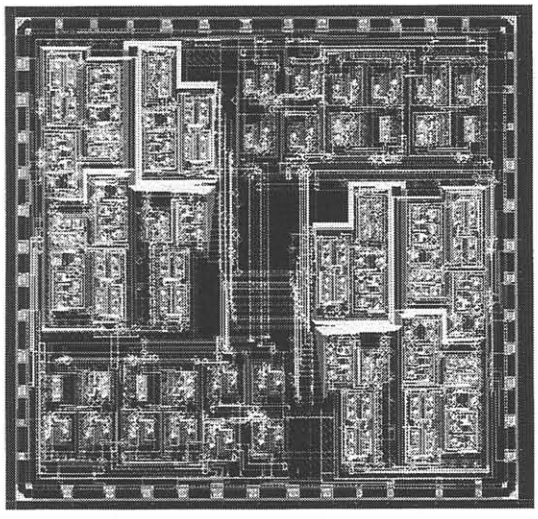

Fig.7 The layout of 8-point FFT LSI. (7mm *7mm)
- Foundry: Austria Mikro Systeme (AMS).
- Broker:Circuit Multi-Projects (CMP)

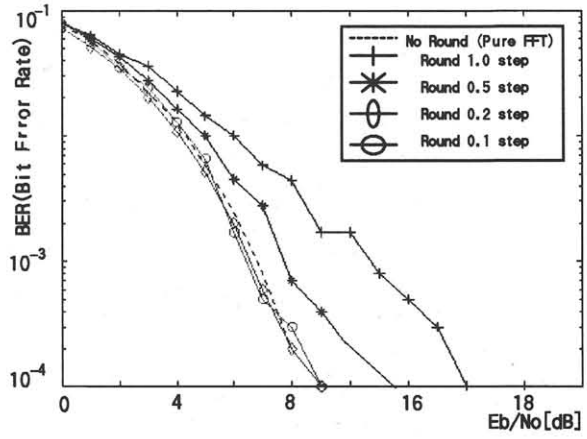

Fig.3 BER estimated by rounding steps.

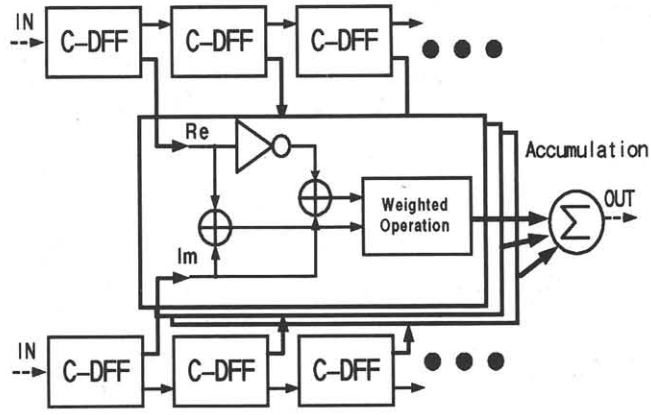

Fig.4 Circuit block diagram of proposed FFT LSI.

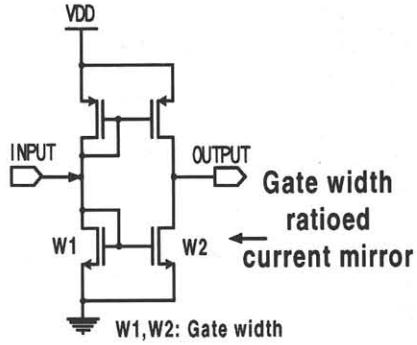

Fig.5 Gate width ratioed current mirror of FFT LSI.

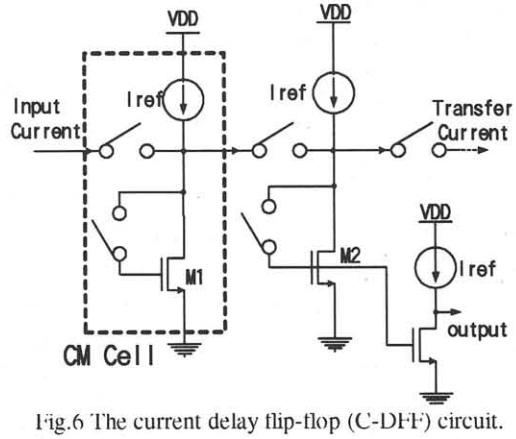

Fig.6 The current delay flip-flop (C-DFF) circuit.