E-6-1 (Invited)

Self-Aligned SiGe HBT Technology for Optical-Fiber-Links and Millimeter-Wave Applications

Katsuyoshi Washio

ULSI Research Department, Central Research Laboratory, Hitachi Ltd. 1-280 Higashi-Koigakubo, Kokubunji, Tokyo 185-8601, Japan Phone: +81-42-323-1111, Fax: +81-42-327-7764, e-mail: washio@crl.hitachi.co.jp

1. Introduction

For future optical communication systems operating at 40 Gb/s and microwave/millimeter-wave systems for wireless communication and intelligent traffic control, high-speed operation and sophisticated functions are required. SiGe HBTs can be fabricated by the well-established Si process compatible with CMOS. A self-aligned selective-epitaxial-growth (SEG) SiGe HBT, which has shallow-trench and dual-deep-trench isolations and Ti-salicide electrodes, has been developed [1]. It has a peak cutoff frequency of 122 GHz, a maximum oscillation frequency of 163 GHz, and a minimum ECL-gate delay of 5.5 ps. A receiver IC chipset, which includes a preamplifier with a 45-GHz bandwidth, and a limiting amplifier with a 32-dB gain, and 1:4 high-sensitivity demultiplexer with a decision circuit, for use in practical 40-Gb/s optical-fiber-link systems has been developed [2]. A dynamic frequency divider with a maximum operating frequency of up to 82.4 GHz for future millimeter-wave systems has also been developed [3].

2. Device Structure and Fabrication Process

A schematic cross-section of a self-aligned SEG SiGe HBT is shown in Fig. 1. The $0.6-\mu$ m-wide SiGe-base/Si-cap multilayer self-aligned to the $0.2-\mu$ m-wide emitter was selectively grown by UHV/CVD. To provide a good link between the intrinsic and extrinsic bases, a poly-Si-assisted self-aligned SEG (PASS) structure was used [4]. As part of the PASS structure, a poly-SiGe base contact simultaneously formed with the SiGe intrinsic base was grown around the buffer poly-Si and beneath the base poly-Si. This self-aligned active-region structure provides both low collector capacitance and low base resistance. Furthermore, to reduce the parasitic capacitances of the collector and substrate, respectively, shallow-trench and dual deep-trench isolations were used. And to reduce the parasitic resistance of all electrodes, Ti-salicide layers were formed.

The SEG layer consists of a 20-nm-thick Si cap, 15-nmthick dual-graded Ge-profile (graded from 0 to 10% and from 10 to 15%) Si_{1-x}Ge_x, 40-nm-thick Si_{0.85}Ge_{0.15}, and 10-nm-thick Ge-retrograded Si_{1-x}Ge_x. A 15-nm-thick 2 x 10¹⁹-cm⁻³ borondoped Si_{1-x}Ge_x layer was formed as the intrinsic base in the SEG layer. The process (except the SEG) to fabricate the SiGe HBTs is almost the same as the 0.2-µm bipolar-CMOS process.

3. Transistor Characteristics

The SiGe HBT with an emitter area of $0.2 \times 2 \mu m^2$ exhibited good I-V performance with a high current gain of 1400. The ideality factor of the base current was 1.15 and the baserecombination current was below 10 pA and the HBT yield, measured from 4000 parallel-connected transistors, was more than 99.9993%. These DC characteristics show that no defects were created in the strained Si/SiGe multilayer during the thermal cycle after low-temperature epitaxial growth.

The low base resistance of 90 Ω , in spite of the short emitter length (2 µm), can be attributed to the highly doped SiGe base and Ti-salicide base electrode. The low collector capacitance of 3.6 fF and low substrate capacitance of 1.8 fF can be attributed to the SiGe HBT with the PASS structure and the shallow-trench and dual deep-trench isolations, respectively. The peak cutoff frequencies and maximum oscillation frequencies of two SiGe HBTs with emitter areas



Fig. 1. Schematic cross-section of a SiGe HBT with Ti-salicide electrodes and shallow-trench and dual-deep-trench isolations.



of 0.2 x 1 and 0.2 x 2 μ m² were 122 and 157 GHz and 122 and 163 GHz, respectively (Fig. 2). The dependence of the gate delay time on the switching current in 53-stage differential ECL ring oscillators for a single-ended voltage swing of 250 mV is shown in Fig. 3. The measured minimum ECL gate-delay time was 5.5 ps at a switching current of 2 mA.

4. IC Performance

As applications of SiGe HBTs, a receiver IC chipset for use in practical 40-Gb/s optical-fiber-link systems and dynamic and static frequency dividers have been developed. A receiver IC chipset includes a preamplifier with a 45-GHz bandwidth (Fig. 4), a limiting amplifier with a 32-dB gain, and 1:4 highsensitivity (40 mVpp) 40-Gb/s demultiplexer with a decision circuit (Fig. 5). These characteristics show that the fabricated ICs are sufficient for use in 40-Gb/s optical receivers. A dynamic frequency divider with a maximum operating frequency of up to 82.4 GHz and a static frequency divider with a maximum operating frequency of up to 60 GHz (Fig. 6) indicate that the self-aligned SiGe HBT technology will also play an important role in future millimeter-wave systems.

5. Summary

A self-aligned selective-epitaxial-growth SiGe HBT was developed. It makes it possible to obtain ultra-high-speed operation – with both f_T of 122 GHz and f_{max} of 166 GHz – and a 5.5-ps gate-delay ECL circuit. A receiver IC chipset for use in practical 40-Gb/s optical-fiber-link systems, including a preamplifier, a limiting amplifier, and 1:4 high-sensitivity demultiplexer, was also been developed. A dynamic frequency divider with a maximum operating frequency of up to 82.4 GHz demonstrates that this SiGe HBT technology can also be applied to millimeter-wave bands.

Acknowledgments

The author thank Drs. A. Anzai, Y. Hatta, and Mr. T. Harada at the Hitachi Device Development Center (DDC) and Drs. O. Kanehisa, K. Seki and Mr. K. Kimura at the Hitachi Central Research Laboratory (CRL) for their encouragement. He also would like to express sincere thanks to Dr. Y. Tamaki, Mr. K. Mikami, and the other process staff members at the DDC for their contributions to the process development. And he thanks his colleagues at the CRL who were part of this work.

References

- K. Washio, M. Kondo, H. Shimamoto, M. Tanabe, E. Ohue, R. Hayami, K. Oda, and T. Harada, in *IEDM Tech. Dig.* (1999) p. 557.
- [2] T. Masuda, K. Ohhata, F. Arakawa, N. Shiramizu, E. Ohue, K. Oda, R. Hayami, M. Tanabe, H. Shimamoto, M. Kondo, T. Harada, and K. Washio, in *ISSCC Digest of Tech. Papers* (2000) p. 60.
- [3] K. Washio, E. Ohue, K. Oda, R. Hayami, M. Tanabe, H. Shimamoto, T. Harada, and M. Kondo, in *ISSCC Digest of Tech. Papers* (2000) p. 210.
- [4] K. Washio, E. Ohue, K. Oda, M. Tanabe, H. Shimamoto, and T. Onai, in *IEDM Tech. Dig.* (1997) p. 795.







