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A Silicon RF-CMOS Class-B Push-Pull Power Amplifier for IMT-2000

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1. Introduction

Recently, bellow-0.1μm level miniaturized Si MOSFETs have been investigated extensively. The transition frequency of over 100GHz has been achieved. This implies that Si MOS devices are applicable to RF application untill ~5GHz in place of conventional GaAs devices. In the 21st-century wireless multi-media, development of low-power mobile terminals is so crucial that all-CMOS system-on-a-chip (SoC) is essentially required.

We are aiming at the low-power low-cost CMOS SoC covering from baseband digital to 2-5GHz RF analog applications. As a preliminary step toward the RF-CMOS, Si analog RF power amplifier (PA) for code-division-multiple-access (CDMA) cellular system has been investigated.[1] The digital cellular systems have been popularized worldwide. Recently in Japan, their prevalency has overtaken that of wired telephone systems. The next-generation wideband CDMA cellular system named IMT-2000 is being developed toward a practical use in 2001. CDMA scheme requires a linear PA in order to preserve an accuracy in modulation and a wide linear dynamic range in transmission-power-control. On the other hand, battery-operated mobile phones demand a high power-added efficiency (PAE) for a long battery life. A trade-off exists between a high-efficiency and high-linearity PA designs for CDMA. Complex hetero-structure GaAs FET-based Class A or AB amplifiers are utilized for the linear operation, while their PAE is ~ 50%[2]. The hetero devices are substantially cost-expensive as compared to silicon devices.

Recently, RF power amplifier composed by Si nMOS devices has been reported[3]. We have reported a CMOS Class-B push-pull amplifier for 900-MHz narrow-band CDMA (IS-95) system.[1] In this paper, a high-efficiency Si CMOS push-pull amplifier is proposed for 1.9-GHz IMT-2000 system. RF-CMOS balancing design is investigated for 0.35-μm MOS devices, and simulation results have shown that PAE of 46% and adjacent-channel-leakage-power-ratio (ACPR) of –44dBc are obtained.

2. RF-CMOS balancing design for 0.35μm n/p MOSFETs

We have studied Class-B n/p push-pull PA. The Class-B operation enables a high PAE compared with Class A or AB operation, and the complementary n/p push-pull circuits lead to a high linearity. The reason why there are few reports on RF complementary-MOS circuits, is considered to be the unbalance in RF characteristic between n- and p-MOSFETs.

Procedures of RF-CMOS balancing design proposed are as follows; (1) both n- and p-channel MOSFETs with various channel widths are fabricated and RF characteristics are measured. (2)RF simulation using the harmonic balance method are performed under various device parameter conditions, and (3)RF-CMOS optimized design for n-/p-MOS push-pull amplifier is determined with paying attention to amplitude and phase of output waveforms.

We have noticed that RF characteristics of n/p-MOS devices are dominated by device parameters such as gate length(L), width(W) and gate/drain biases(V_G,V_D). Though adjustments of L in nMOS and those of W in pMOS have been investigated in Ref.[1], longer channel length of nMOS is accompanied with degradation of gain, resulting in poor performance for higher frequency and power operation. Here, adjustments of W in nMOS and those of V_G in pMOS are investigated as RF-CMOS design for IMT-2000.

Si devices fabricated are 0.35-μm gate-length normal poly-Si-gate MOS devices using a mixed-signal CMOS process. Figure 1 shows a schematic of the fabricated MOSFETs. Device parameters of n- and p- MOSFETs are listed in Table I. The output characteristics of n- and p-MOSFETs are shown in Figs. 2(a) and 2(b), respectively. Solid lines indicate the measured results. Gate bias is set to be a threshold voltage, i.e., Class-B operation. PAEs of 54% and 40% are obtained at 1950MHz in n- and p-MOSFETs, respectively. Doted lines indicate the simulation results using BSIM3v3 model parameters.

Through RF harmonic balance simulations, balancing design has been optimized for push-pull operation. Amplitude and phase of output waveforms are noticed. Figure 3(a) shows the dependence of MOSFET gain on channel width in nMOSFET, while Fig. 3(b) that on gate bias in pMOSFET. In this case, the amplitude of both n- and p-MOSFET is mainly tailored. The optimized parameters are as follows; channel width of nMOS is 30μmX100=3000μm for nMOSFET, gate bias of pMOSFET is –0.8V, a little higher than threshold voltage of -0.6V. Drain biases are 3.3V and –3.3V for n- and p-MOS devices, respectively.

3. Complementary Push-Pull Operation Simulation

Based on the simulated data in Figs. 3, a performance of n/p push-pull amplifier is evaluated. Figure 4 shows the simulated output characteristics of n/p push-pull device with the balancing design. Power divider and combiner are assumed to be ideally loss-less in the simulation. A spurious radiation has been sufficiently suppressed, and ACPR has been also suppressed down to –44dBc@5MHz-offset. The maximum PAE has been found to be as high as 46%@16dBm@1.9GHz/QPSK-modulation. This meets the specification of IMT-2000. After RF-CMOS balancing design, high PAE and low ACPR are obtained in n/p push-pull amplifier.

4. Conclusion

Si RF-CMOS Class-B push-pull amplifier is proposed for the next generation wideband-CDMA (IMT-2000). RF-CMOS balancing design has been investigated and the simulated maximum PAE of 46% have been attained. Si RF-CMOS has a potential to realize all-silicon CMOS system on a chip for wireless multimedia.

References: 1. M. Yokoyama, et al.,Ext. abst. 1999 SSDM, p.572 2. T.B.Nishimura, et al., IEEE MTT-S Int. Microwave Symp. Dig. (1999) p.WE3A-2. 3. I. Yoshida, et al., Tech. Dig. of IEDM 1997, p.51.

Table I. Device parameters

Channel length:	0.35μm
Channel width:	1200 - 7200μm
Supply voltage:	3.3V(nMOS), -3.3V(pMOS)
Threshold voltage:	0.6V(nMOS), -0.6V(pMOS)

Technology: Austria Micro Systems 0.35μm CMOS

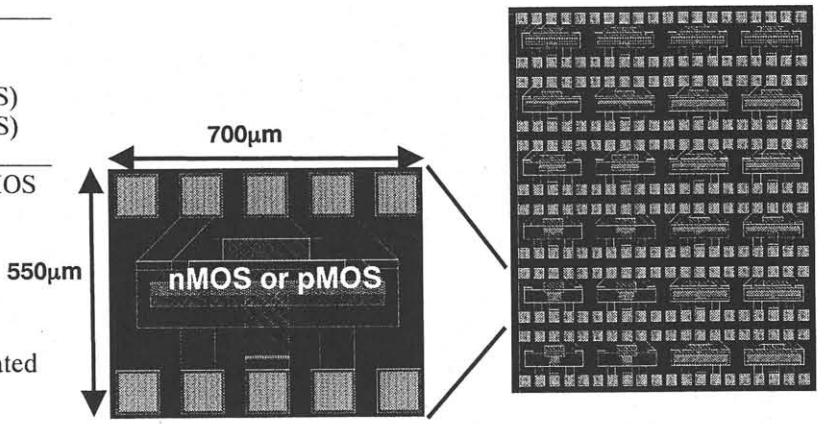


Fig.1 Schematic of the fabricated MOSFETs

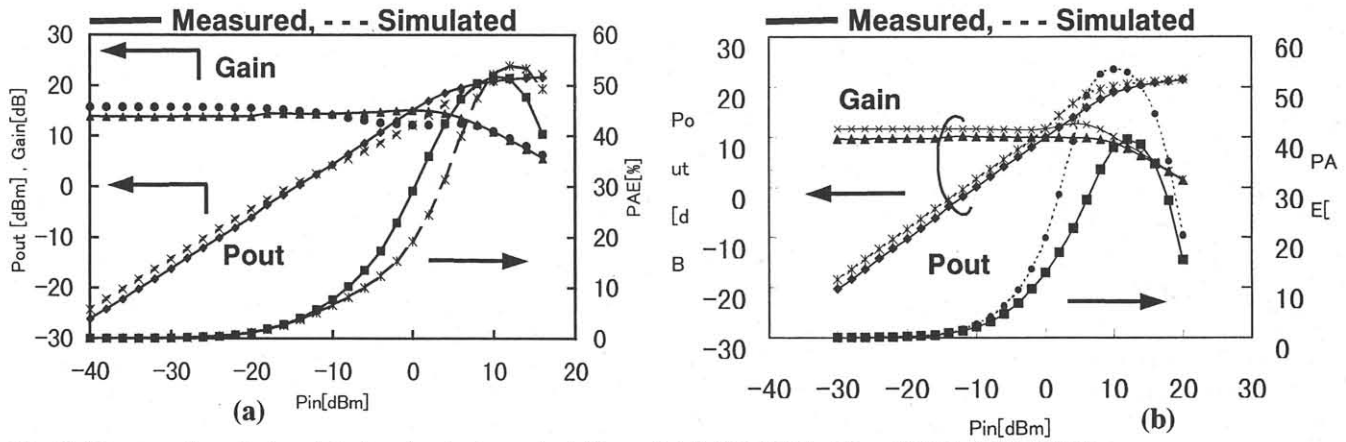
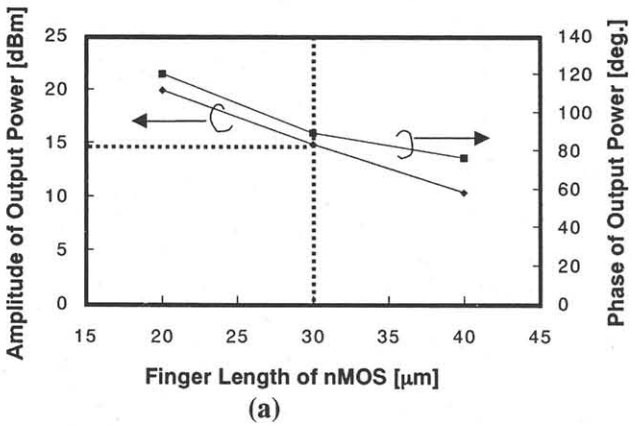


Fig.2 Measured and simulated output characteristics of (a)nMOS(W=10μmX120, VG=0.7V) and (b)pMOSFET(W=20μmX120, VG=-0.9V). L=0.35μm, VDD=|3.3V|.



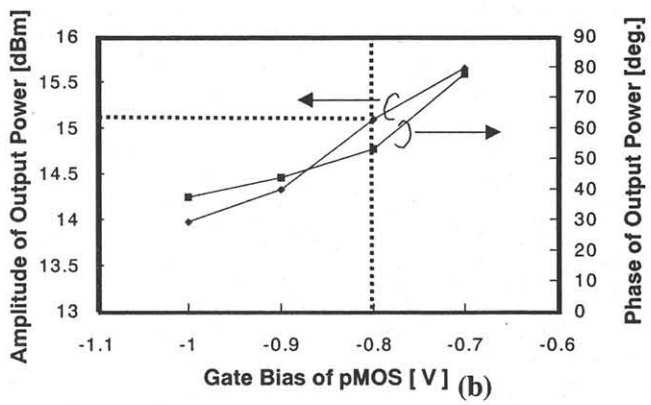


Fig.3 Simulated characteristics for RF-CMOS balancing (a)amplitude, phase vs. channel width in nMOS and (b) amplitude, phase vs. gate biases in pMOS devices. Input power is 4dBm

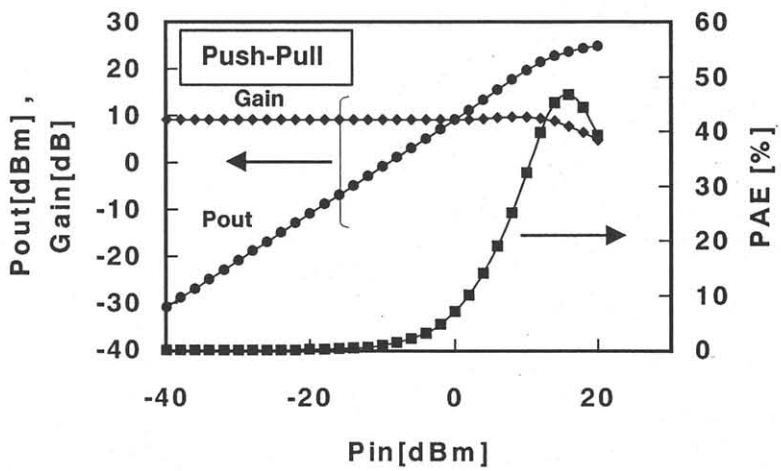


Fig. 4 Simulated output characteristics of n/p push-pull amplifier at 1.95GHz.
nMOS;W=30μmX100, VG=0.6V
pMOS;W=10μmX300, VG=-0.8V