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Plasma Charging Damage Immunity in SOI Devices

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Abstract: Plasma charging damage is very critical in ULSI technology with continuously shrinking dimensions. Very little work has been reported to understand such effects in high performance SOI technology. This paper focuses on a detailed evaluation of plasma charging damage in SOI devices with full-flow back end process. Both classical antennas and SOI-specific differential antenna, connected to the gate and S/D diffusion, have been studied. Our data indicate that SOI devices are substantially more robust to plasma charging damage than bulk silicon devices. Direct experimental evidence determined that any contact of a MOS device to the back substrate induces significant gate oxide charging damage.

Introduction: A high performance 0.18 um technology on SOI substrate with copper metallization and low ε FSG dielectric has recently been reported [1]. The test chip built using this technology has demonstrated microprocessor performance above 1 GHz. Plasma charge damage has been evaluated on such high performance SOI CMOS technology.

Plasma charge is collected only at the gate terminal in the bulk silicon technology, as this is the only floating node. However, in SOI technology, the presence of the buried oxide floats both that gate and diffusion nodes. Thus, plasma charge may accumulate at both the gate & S/D diffusion node antennas. A differential between these two, charges may cause flow of damaging current through the gate oxide. Previous work [2] has investigated plasma damage to N-MOS SOI built with thicker gate dielectric. This study considers gate dielectrics in the 2.0 to 2.5nm range, where tunneling current can modify the balance between the two floating nodes. Further, we investigate the plasma damage associated with the fabrication of a high performance damascene Cu BEOL and body to substrate contacts. Such effects are evaluated for realistic antenna situations on the chip and their potential impact on the gate oxide is studied.

Experimental: Bulk silicon wafers have been processed together with the SOI wafers in the same lot using the same mask set. All the antenna structures are full flow with polysilicon, local interconnect, seven metal and all the via antenna levels. The polysilicon and metal antenna levels are stacked finger type structures with minimum allowed pitch and are connected by via antenna arrays of minimum allowed via dimensions to evaluate the worst case charge damage. The test structures are both P-MOS and N-MOS transistors of 0.3 μm x 20 μm and 0.18 μm x 20 μm dimensions with gate oxide thickness ranging from 2.0 to 2.5 nm.

Results and discussions: The gate leakage current is found to be the most convenient and equally sensitive parameter for detecting plasma charging damage in 2.0 to 2.5 nm gate oxides (Fig. 1). The Time Dependent Dielectric Breakdown (TDDB) measurements (Fig. 3) and ramp breakdown voltage measurements (Fig. 2) also correlates well to the plasma damage caused gate leakage signature. Figure 4 shows gate leakage current distributions for large classical antenna (gate antenna only) devices fabricated on bulk silicon and SOI wafers. This plot clearly shows that the SOI devices are substantially more robust against plasma charging damage compared to those on the bulk silicon wafer. SOI devices even show less damage than bulk devices with protect diodes. TDDB comparison of SOI antenna devices to reference device is shown in the Fig. 5, further confirming no damage to the gate oxide. The SOI devices suffer no degradation since the plasma charge collected from the gate antenna can not create damaging tunneling currents as the device is isolated from the back substrate by the buried oxide.

In a SOI device, antennas may be connected to both the gate and diffusion nodes. These antennas can charge to different voltages depending upon their collection areas, resulting in tunneling currents through the gate oxide, as shown in Figure 6. In order to evaluate such effects, SOI specific antenna structures have been designed in which full flow antennas of three ratios are connected in various combinations (Table 1) to the gate and the S/D diffusion terminals of the SOI device. Fig. 7 shows the gate leakage current distribution in P-FET and N-FET devices across 8 wafers for all the SOI-specific differential antenna configurations. Breakdown voltage distribution for a typical differential antenna device and reference device is shown in the Fig. 8. These results clearly indicate that SOI devices are essentially immune to the plasma damage in these configurations where ratios of gate and diffusion antenna is up to 3. The classical antenna (Fig. 4 & Fig. 5) device also has a small antenna associated with S/D diffusion contact pads, which is 50 times smaller than the gate antenna. The immunity of these devices to damage may be related to the quick charging of body due to the gate tunneling current.

In order to simulate bulk silicon charging damage conditions on SOI wafers, structures have been fabricated with the gate and the diffusion terminals selectively connected to the back side silicon substrate. These connections are created by etching through the buried oxide and filling it with highly doped polysilicon before all metal and via processes. A device with large antennas to both the gate and the diffusion terminals which shows no charging damage when floating is found to get heavily damaged when either S/D diffusion node or gate node is connected to the back side substrate (Fig. 9 and Fig. 10). These results clearly show that the plasma charging damage to a SOI device can occur from either the gate or the diffusion antennas. Isolating the device from the back substrate in SOI technology make them inherently robust against charging damage.

Conclusion: SOI devices exhibit highly robust behavior against plasma charging damage when evaluated using full-flow classical antennas and new SOI specific differential antennas. The isolation of the SOI devices from the back substrate is shown as the main reason for their immunity to plasma charging damage.

References:

[1] E. Leobandung et al., IEDM Tech. Dig., pp. 679, 1999.
[2] T. Poiroux et al., IEDM Tech Dig., pp. 97, 1999

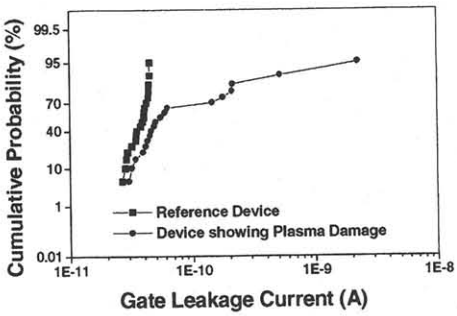

Fig. 1: Gate Leakage current distribution on reference and plasma damaged devices.

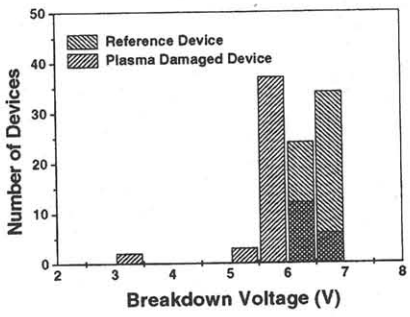

Fig. 2: Breakdown voltage comparison between reference and plasma damaged devices.

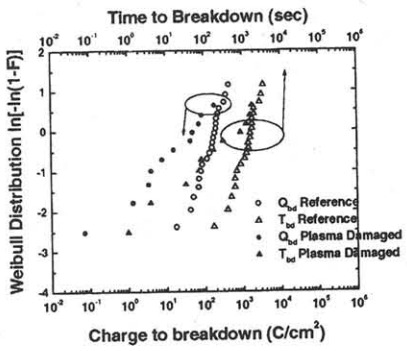

Fig. 3: TDDB comparison between reference and plasma damaged devices.

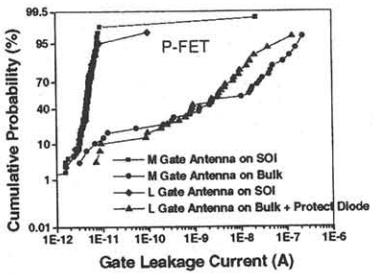

Fig. 4: Gate leakage comparison between bulk and SOI devices with classical antenna.

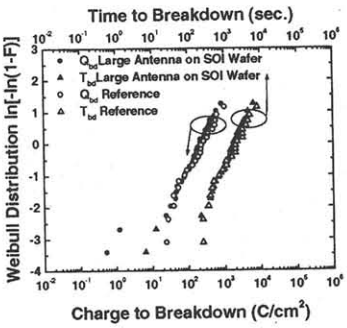

Fig. 5: TDDB comparison between reference and antenna devices in SOI wafer.

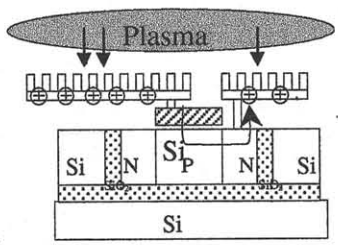

Fig. 6: Schematic showing plasma charge damage mechanism in SOI device.

Gate	Diffusion
Large (L)	Large (L)
Large (L)	Small (S)
Small (S)	Large (L)
Large (L)	Medium (M)
Medium (M)	Small (S)

Antenna Ratios:
Large = 2 x Medium
= 3 x Small
= 50 x Pads

Table 1: Various combinations of antenna connected to the gate and diffusion in SOI device.

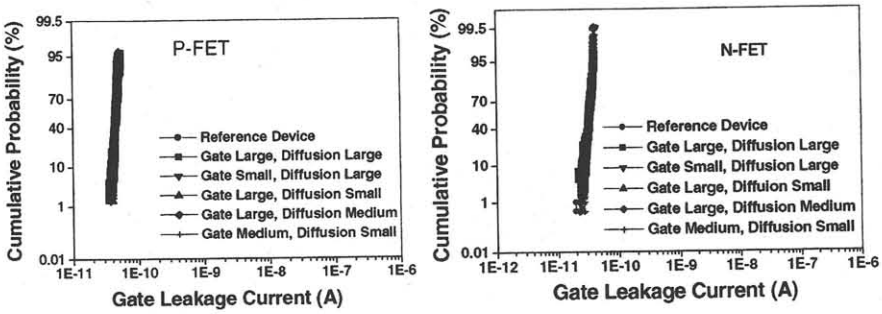

Fig. 7: Gate leakage current distribution of SOI antenna devices with various combinations of antenna connected to gate and diffusion.

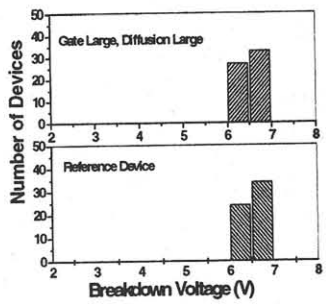

Fig. 8: Breakdown histogram of typical SOI antenna and reference devices.

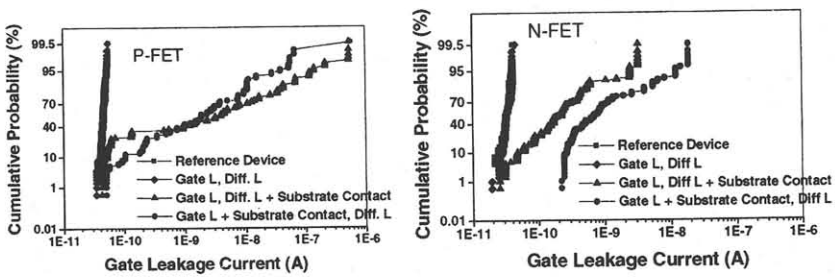

Fig. 9: Gate leakage current distribution of reference devices, floating SOI antenna devices and SOI antenna devices with either diffusion or gate connected to back substrate.

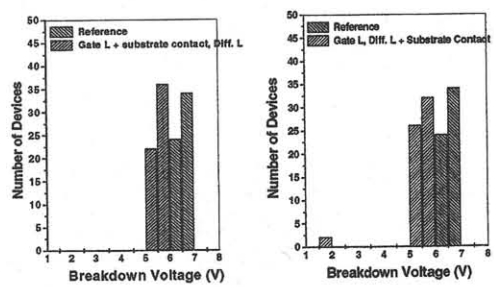

Fig. 10: Breakdown voltage distribution of SOI antenna devices with and without connection to the back substrate.