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Endurance Enhancement in *micro*FLASH® Memory Device

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1. Abstract

The *micro*FLASH® (NROM™) concept is a 2 bit memory cell using an ONO dielectric as a storage media.
To establish the capabilities and applications of the technology, endurance tests were performed on a 2Mb device. No limitation was found to cycle the device to 100,000 cycles and beyond.
The *micro*FLASH process has been qualified and implemented in production for applications requiring a limited number of program-erase cycles. The objective of the described work was to significantly increase the number of cycles. R&D is in progress to qualify the device for 10,000 cycles.

2. Introduction

Non Volatile Memory (NVM) has a wide spectrum of applications, ranging from a one time programming (OTP) for data code to a "million" programming and erase cycles for data storage. Today the most common technology uses a polysilicon layer as a floating gate (FG).
The *micro*FLASH process, that utilizes Saifun NROM technology developed by Dr. Boaz Eitan [1], (see box attached) and provides a cost-effective alternative to the FG technology.
From Figure#1, one can easily see that there is no over erase in the *micro*FLASH cell. Since electrons trapped in the nitride assist in hot hole vertical acceleration, the erase is self-limited. Over programming might cause electrons to get trapped in the ONO layer above the channel far from the junction edge thus increase erase time, This phenomenon indicates the endurance window closure. Single cell (test chip) cycling data is shown in Figure #3.
In a full device array, endurance degradation is expressed as an increase in erase pulse count. Programming time in average does not change.

The *micro*FLASH® cell is an n-channel MOSFET device where the gate dielectric is replaced by an ONO (Figure #2). Buried diffusion Bit Lines are crossed by polysilicon Word Lines in a fieldless array. The cell is programmed by Channel Hot Electron injection. Electrons are locally stored in the nitride self aligned to the n^+/p^- junction.
Read is done in *"reverse"* direction relative to programming, by switching source/drain positions. This technology increases memory storage size with two physically separated bits per cell. The second Bit is programmed and read by interchanging the two junctions.
Erase involves Tunneling Enhanced Hot Hole injection. Hole flux is generated by a Band-to-Band tunneling.
The process and operating principles of the *micro*FLASH cell were presented previously [2,3].

3. Endurance Optimization.

The work done to improve endurance on the 2Mb *micro*FLASH product is described below:
A theoretical model was proposed to describe the transistor operation during programming and erase. Simulation work was done, using SUPREM-4 for 2D doping concentration calculation. Several approaches to modify the junction's edge implant conditions (dose, energy, species, thermal cycle etc.) were used as input parameter. Figure #4 shows a simulation result from one of the experiments.
After the initial simulation screen, several experiments were processed on the 2Mb device wafers. Single cell parameters of the experiment wafers were measured and plotted. Some measurements were done in extreme conditions. Figure #5 shows cycling's Vt window in the experiment range.
Several wafers were assembled and parts were cycled using a standard commercial cycling tester, and the best process option was chosen.

4. Endurance Results.

Before this optimization work the number of programming/erase cycles was limited. With the new drain junction conditions the product could be cycled to more than 100,000 program/erase cycles. Figure #6 shows the number of erase pulses, before the optimization and after the optimization, where the number of pulses stabilizes at a low level. It shows that there was no physical degradation in cycling.

5. Summary

Drain engineering was the main factor for achieving a large number of cycles.

Endurance in common memory devices is limited by physical degradation of the memory cell (leakage current through the dielectrics). In the *micro*FLASH technology this mechanism is not evident in the operation range tested.

This engineering work was a part of a methodological process of modeling, simulation and verification that helped develop control and predictability of the manufacturing process.

The *micro*FLASH device, based on a two-bit localized trapping concept, is a paradigm shift in non-volatile memory to replace standard EPROMs FG brands.

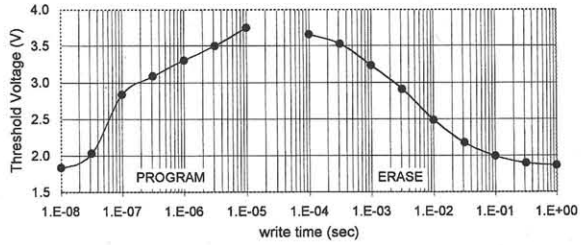

Figure # 1: Program and Erase curves of a single cell. Erase Vt stabilizes with time, but Programming Vt can continue to increase

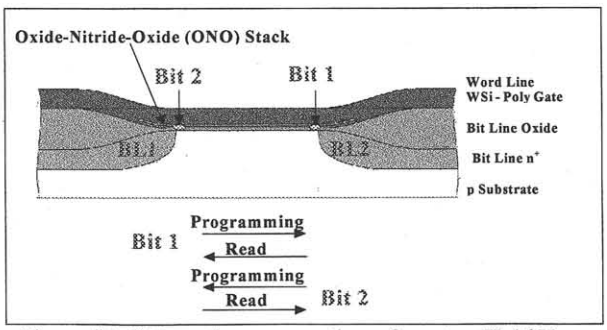

Figure #2: Schematic cross-section of a *micro*FLASH cell showing the two physically separated bits.

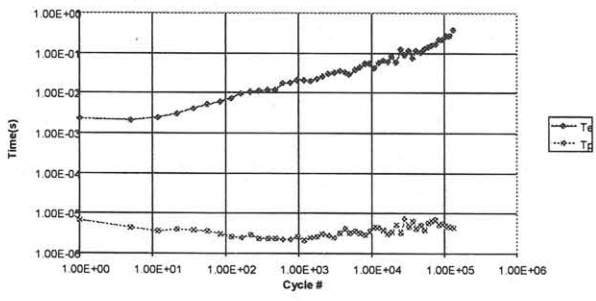

Figure # 3: Window closure, before the optimization work was performed. The Figure presents a single cell (test chip) behavior. The erase time increases (degrades) while programming time does not change in course of cycling

References

[1] B. Eitan, U.S: Patent No. 5,768,192 "Non-volatile semiconductor memory cell utilizing asymmetrical charge trapping", Jun. 16, 1998.

[2] E. Koltin et al "Enabling Technology for Embedding Flash Memory in System-on-Chip Applications" Electronic Parts and Materials Kogyo Chosakai Publishing Co., Ltd June 2000 Page # : pp.20-25

[3] B. Eitan, et al. "Can NROM, a 2-bit trapping storage cell, give a real challenge to floating gate cells?" Proc. SSDM 99, Tokyo, Japan, pp. 522-524, Sept. 1999

[1] *Micro*FLASH® is a registered trademark of Tower Semiconductor Ltd. Saifun NROM ™ is a trademark of Saifun Semiconductor Ltd.

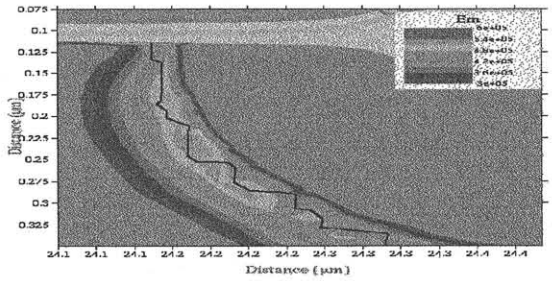

Figure #4: Simulation of certain process conditions and operating potential. Shows electrical fields formed at the junction edge.

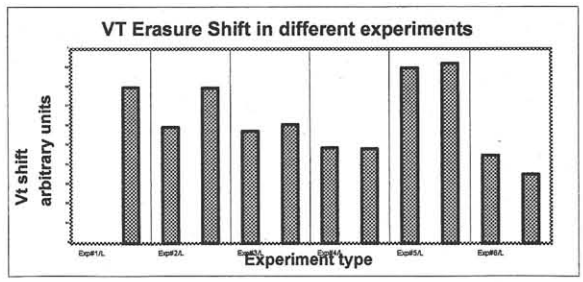

Figure #5: Experimental lot results, show window closure in different drain engineering conditions. Analysis was done in high/low measurements levels, to enhance the differences

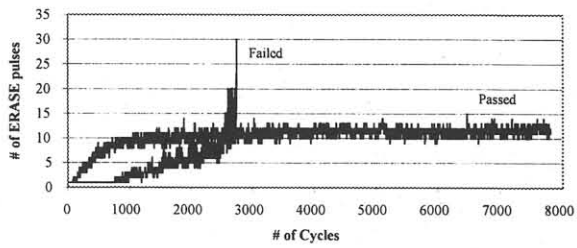

Figure #6: Number of erase pulses provided to erase a 2Mb part during cycles. Failure criterion is 30 pulses. As a refernce to the optimized process, a different part from another experiment shows failure