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Fabrication and Characterization of Pt/(Bi, La)$_4$Ti$_3$O$_{12}$/Si$_3$N$_4$/Si MFIS Structure for FET-Type Ferroelectric Memory Applications

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1. Introduction

Recently, much attention has been paid to $(Bi,La)_4Ti_3O_{12}$ (BLT) films for nonvolatile ferroelectric memory appli-cations[1]. For FET-type ferroelectric memories, a ferro-electric film with a small remanent polarization is necessary. In this work, a c-axis-oriented BLT film, which has a remanent polarization P_r as small as 4 μ C/cm^2 has been investigated. BLT films were formed by the sol-gel method on Si_3N_4/Si substrates under various growth conditions. The amorphous Si_3N_4 (2-3 nm) film was formed by using atomic nitrogen radicals [2].

2. Fabrication of c-axis Oriented BLT Films

Using stoichiometric $(Bi_{3.25}La_{0.75}Ti_3O_{12})$ sol-gel solution, no X-ray diffraction (XRD) peak was observed in the BLT films when the annealing was performed at temperatures lower than 800 ℃ in O_2 ambient. To enhance the cry-stallization of the BLT films on Si_3N_4/Si, 2.5 to 7.5% Bi-excess solutions were used and the thickness of BLT film was optimized at 75nm for a single spin-coating process. A weak BLT(006) peak was observed in XRD pattern at a crystallization temperature of 800℃ when the excess-Bi was more than 5% (Fig.1). It was also found that the crystallization temperature was significantly reduced when the samples were annealed in air. As shown in Fig.1, the BLT(006) peak was observed even when the annealing temperature was 600°C, which was 200°C lower than crystallization in O_2 ambient. Moreover, when the crystallization was performed at 800°C in air, relatively large BLT(006) peak was observed, regardless of the Bi content in the precursors. Figure 2 shows typical cross section and surface morphology of the BLT film observed by scanning electron microscopy. As can be seen in the film, sharp interface and good surface morphology were obtained.

3. Pt/BLT/Si$_3$N$_4$/Si MFIS Structures

From the previous consideration, BLT/Si_3N_4/Si structures were formed by annealing the BLT films at 800°C in air. In order to obtain desired electrical properties, it is important to control crystalline orientations of the BLT because BLT has a large anisotropy in dielectric and ferroelectric properties. For instance, the remanent polarization and coercive field for $Bi_4Ti_3O_{12}$ are 50 μ C/cm^2 and 50kV/cm along a-axis, respectively, whereas those are only 4 μ C/cm^2 and 4kV/cm along c-axis, respectively. As shown in Fig.3, a completely c-axis oriented BLT film was obtained when the film was pre-annealed at 400°C. When the film was pre-annealed at 500°C, randomly oriented BLT film including (117) crystallites was obtained. This is presumably related to the result of our previous work, which shows that the crystallization starts at 500°C for MOCVD-grown $Bi_4Ti_3O_{12}$ films [3].

Next, we measured the capacitance-voltage (C-V) characteristics of the Pt/75nm-BLT/3nm-Si_3N_4/Si MFIS (Metal/Ferroelectric/Insulator/Semiconductor) structure were measured. The c-axis oriented film showed a good C-V hysteresis property with a memory window of about 1V for a voltage sweep of ±5V, as shown in Fig.4. On the other hand, if a BLT film which contained (117) crystallites was used, almost no observable memory window was obtained for a voltage sweep of ±5V. When the randomly oriented BLT film is used, only small minor loop can be used because the remanent polarization of the film is too large. On the other hand, since the c-axis oriented BLT film has a small remanent polarization, a saturated (or almost saturated) P-E loop can be used in the MFIS structure. Hence, larger memory window can be obtained with a c-axis oriented BLT film.

In addition, it is found that the accumulation capacitance of the MFIS structure with the BLT film containing (117) crystallites is smaller than that of the MFIS structure with the c-axis oriented BLT film. This result seems to be contradictory to the generally known fact that a (117) oriented BLT film has a higher dielectric constant than a c-axis oriented BLT film. However, this result can also be explained by the fact that only a minor loop in the P-E characteristics is used in the sample shown in Fig.4(b), since an equivalent dielectric constant along a minor loop is much smaller than that along a saturated loop. Therefore, it can be concluded that a c-axis oriented BLT film is suitable for the MFIS-FET applications.

Next, we fabricated Pt/BLT/Si_3N_4/Si MFIS structures with a 150-nm-thick BLT film to obtain a large memory window. Crystallization was carried out at 800°C in air. As shown in Fig.5, XRD peak intensities were doubled for the 150-nm-thick BLT film compared to those for a 75-nm-thick film. It was also found from the C-V characteristics shown in Fig.6 that a memory window of 2 V was obtained when the BLT thickness was 150 nm, which was twice of the memory window obtained for the MFIS structure with a 75-nm-thick BLT film.

4. Conclusion

C-axis oriented BLT films were successfully formed on

Si_3N_4/Si substrates using Bi-excess solutions. By annealing the films in air, crystallization temperatures were formed to be reduced to 600°C. Furthermore, the Pt/BLT/Si_3N_4/Si MFIS structures exhibited good C-V characteristics with memory windows of 1 and 2V for a voltage sweep of ±5V when the BLT thicknesses were 75 and 150nm, respectively.

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References

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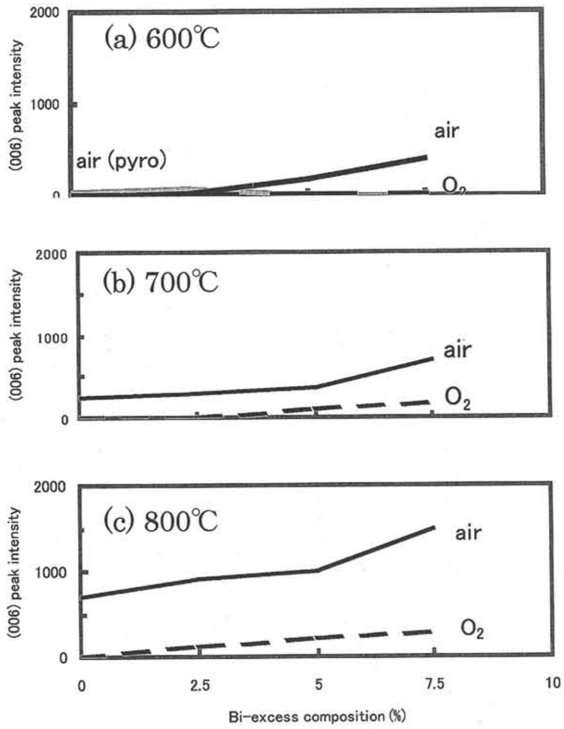

Fig.1 Relationships between Bi-excess composition and XRD (006) peak intensity. (a)600℃ (b)700℃ (c)800℃

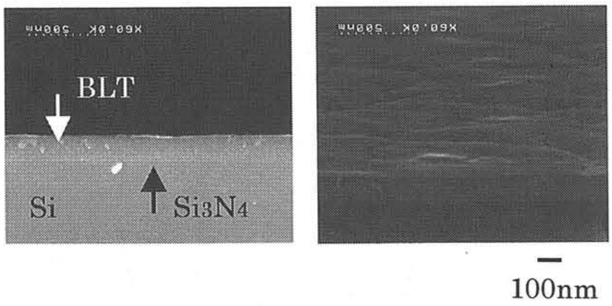

Fig.2 Surface morphology of BLT film on Si3N4

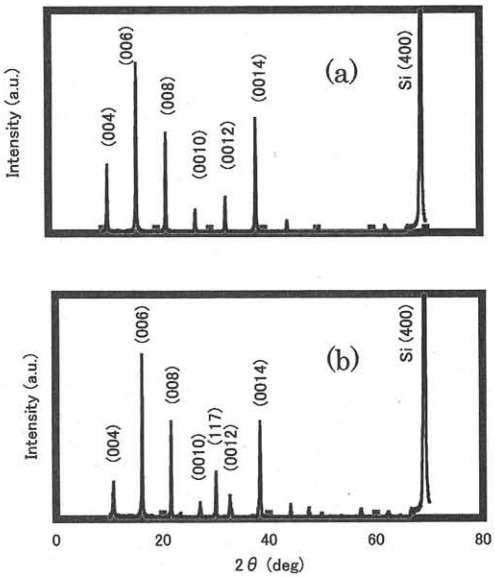

Fig.3 XRD patterns of BLT films. (a) c-axis orientation (b) random orientation

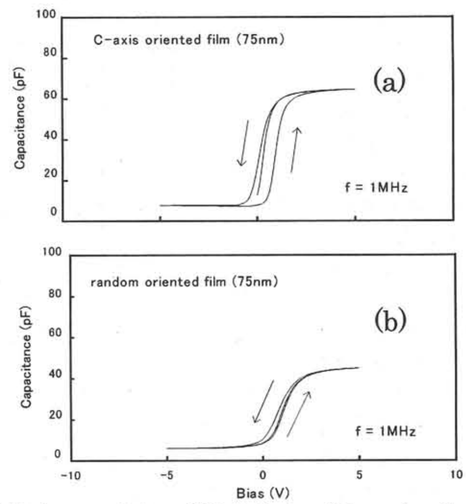

Fig.4 C-V characteristics of BLT diodes. (a) c-axis orientation (b) random orientation

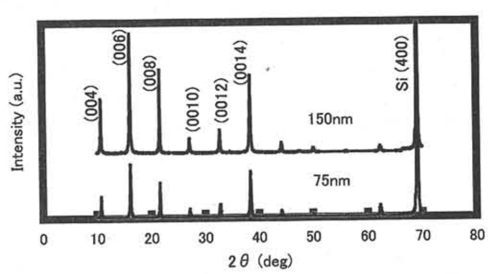

Fig.5 XRD patterns of BLT films with different thicknesses.

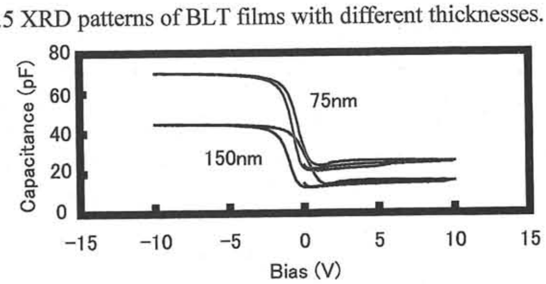

Fig.6 C-V characteristics of BLT films with different thicknesses.