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A Vertical, MOS-Based Silicon Tunneling Transistor

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Abstract

A vertical, MOS-gated tunneling transistor in silicon is fabricated. Pronounced transistor action due to Esaki tunneling is demonstrated at room temperature. At a low supply voltage of -0.2V a current gain greater than 4 orders of magnitude with saturation behaviour is achieved.

Introduction

Tunneling devices are thought to be possible candidates for post silicon MOSFETs. Increase in speed by quantum-mechanical tunneling is one benefit, but also higher functionality of quantum devices is an advantage. A rich spectrum of possible tunneling transistors is proposed and fabricated in various materials and heterostructures. Although several of these devices are quite successful according to some (but not all) benchmarks, none has found large-scale commercial application for general-purpose in digital and analog electronics to date. High volume production should be based on silicon to match well with existing conventional logic circuitry. Based on our vertical MOSFET technology [1] we modified the fabrication process to establish gate-controlled Esaki tunneling for transistor action in a silicon device.

Device Fabrication

The device structure consists of a MOS-gated pin diode proposed by *Quinn et al.* [2] to study the physics of a two-dimensional electron channel. As a parasitic effect, the so-called GIDL, the tunneling behavior in commercial devices was identified in earlier DRAM cells (TTC) by *Banerjee et al* [3]. *Koga and Toriumi* [4] fabricated such a device in planar technology on SIMOX wafers and were focused on the demonstration of a negative differential conductance (NDC) in forward direction at room temperature. To achieve good transistor action with high tunneling performance we fabricated a vertical, MOS-gated pin structure as depicted in Fig.1. On a highly n^+-doped substrate (acting as source) 100nm intrinsic silicon was deposited. The top region (drain) was formed by the deposition of a 3nm thin, highly boron doped layer and 300nm p^+-contact region. The grown layer system was mesa-etched, gate oxide with thickness of 20nm was grown and covered with n^+-poly-silicon. The gates were patterned, isolated with LPCVD nitride and metallized with Al.

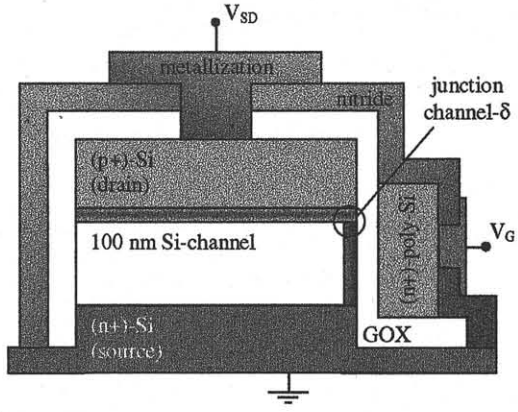

Fig.1: Schematic sketch of the Esaki-FET.

Simulations

Without gate voltage the vertical structure acts as a pin diode where the p^+-and n^+-region are separated by 100 nm intrinsic silicon. This I-V characteristics is indicated in the simulation (Fig.2) by open squares.

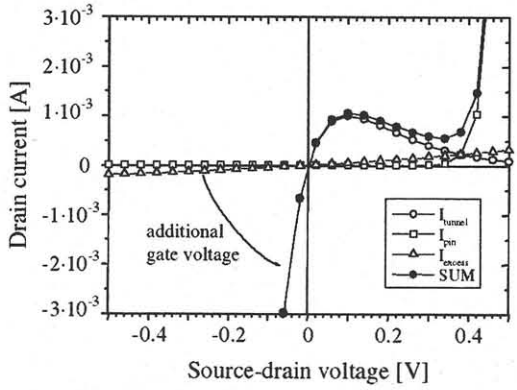

Fig.2: Simulation of an ideal Esaki-FET predicted by a simple tunneling model. The contributions of pin diode, tunneling current and excess current are shown as open symboles.

By applying a positive gate voltage an electron channel is influenced beneath the gate oxide as in a conventional MOSFET. The contact region between the n^+-channel and the p^+-drain now forms a band-band tunneling barrier like an

Esaki diode. The amount of electrons supported by the channel and the tunneling region can be controlled by the MOS gate field. Although due to the silicon band structure the change in I-V characteristics is expected to be small in forward direction, significant transistor action is enabled in reverse direction.

Experimental Results

Experimental I-V characteristics are shown in Fig.3 to Fig.6. In Fig.3 the predicted control by the MOS gate bias can be seen.

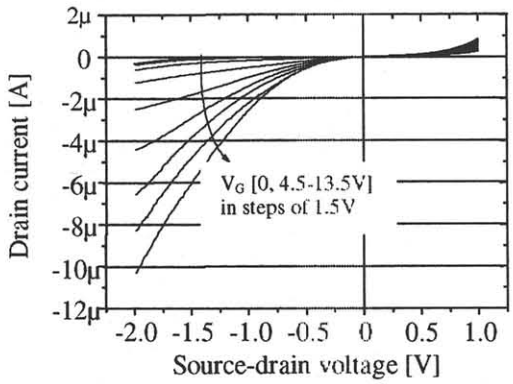

Fig.3: Experimental output characteristics for a device with a drain doping of around $4 \cdot 10^{19} cm^{-3}$.

The input I-V characteristics of this device is shown in Fig.4. For low values of supply voltage (V_{SD}=-0.2V) the gate controlled current gain amounts to 3 orders of magnitude.

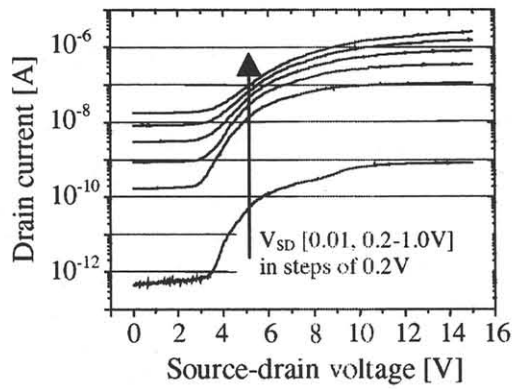

Fig.4: Experimental transfer characteristics for a device with a drain doping of around $4 \cdot 10^{19} cm^{-3}$.

The "threshold voltage" for tunneling is about V_G~3V, which is dependent on channel doping, oxide thickness and the actual electric field in the tunnel region. The saturation behaviour is clearly developed.
In Fig.5 the characteristics of a device with increased p^+-doping is shown. In this case the drain region is started with an ultra-highly doped 3nm layer with a doping amount of $2.6 \cdot 10^{14} cm^{-2}$.

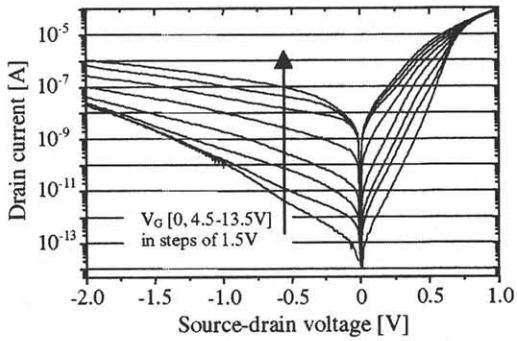

Fig.5: Experimental output characteristics for a device with ultra-high start drain doping ($2.6 \cdot 10^{14} cm^{-2}$).

Now a remarkable current gain of more than 4 orders of magnitude by applying a gate-voltage is achieved. After subtraction of the bulk current the gate controlled channel current is depicted in Fig.6. The NDC appears around 0.6V due to series resistances.

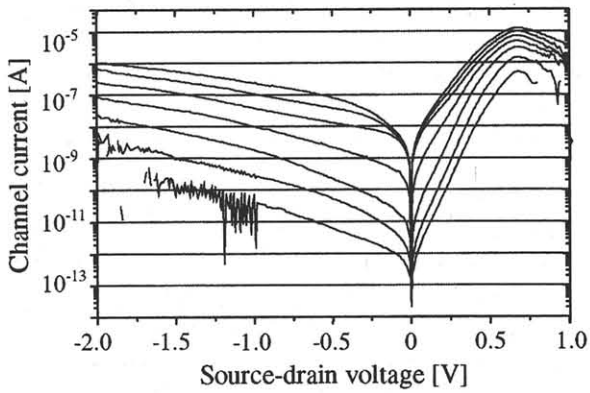

Fig.6: Experimental gate controlled channel current for a device with ultra-high start drain doping ($2.6 \cdot 10^{14} cm^{-2}$).

Conclusion

First measurements on the fabricated vertical Esaki-FETs exhibit several advantages for future ULSI: MOS gate control without steady-state current consumption, fast switching due to exponentional increase of current with gate voltage, safe on/off switching at very low voltage levels and very low leakage currents (pA/μm). In addition the future problem concerning oxide thickness and channel doping fluctuations is more relaxed compared to MOSFETs with similar channel lengths. Because classical electron transport (drift-diffusion) and quantum-mechanical transport (band-band tunneling) are realized simultaneously the presented device may be an ideal candidate to step over to post-MOSFET devices.

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