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LE-2-2

# Performance of Submicron Large-Grain Polysilicon-on-Insulator (LPSOI) MOSFETs Formed by Crystallization of Amorphous Silicon

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## 1. Introduction:

SOI technology provides flexibility for designing novel devices as it removes the restrictions to have transistors stay on top of the single crystal silicon bulk. Some examples are DTMOS and Double-gated MOSFET. It also allows the fabrication of multi-film stacked 3-D transistor circuits. To achieve the ultimate flexibility make available from SOI technology, a method to form high quality silicon film on oxide is required. Some proposed method include wafer bonding [1] and various lateral crystallization method [2,3]. We have previously demonstrated that with the combination of MILC and high temperature annealing on amorphous film, very large grain polysilicon can be achieved [2]. MOSFETs fabricated on these Large-grain Polysilicon SOI (LPSOI) film demonstrate near-SOI MOSFET performance. In this paper, true SOI performance submicron LPSOI MOSFET is reported. A detail study on the characteristics of submicron LPSOI MOSFETs, including short channel effect, device variations and design strategies is presented.

## 2. Crystallization and Device Fabrication:

The formation of LPSOI MOSFET starts with growing 3000Å of oxide on normal silicon wafer. 1000Å of amorphous silicon was then deposited at 550°C, followed by 3000Å of LTO, in which the seeding window are patterned next to the desired region for crystallization. 100Å of Ni was then deposited and lateral crystallization was carried out subsequently at 560°C for 20 hours in $N_2$ ambient. The remaining Ni and LTO were removed. The wafers were subsequently annealed at 900°C for 30 min in $N_2$ ambient to enlarge the silicon grains to several tens of microns through secondary grain crystallization. Finally, conventional SOI CMOS process was used to fabricate the LPSOI MOSFETs on the selected area. The thickness of gate oxide is 110Å. The critical steps are illustrated in Fig.1. The LPSOI process is compatible with conventional SOI CMOS technology, with only one extra mask added for the seed window definition.

## 3. Device Performance:

Fig.2 and Fig.3 show the subthreshold and $I_d$-$V_d$ characteristics of n-channel and p-channel LPSOI MOSFETs with $L_G$=0.4μm and 0.5μm respectively. The submicron LPSOI MOSFETs exhibit very good characteristics, including a subthreshold slope of 72mV/dec, a $g_m$ of 198mS/mm and an $I_{dsat}$ of 0.25mA/μm at $V_g$=1.3V for NMOS, which is comparable to MOSFETs fabricated on single crystal silicon and much better than other reported high temperature TFTs developed for 3-D circuit application [3]. The extracted LPSOI MOSFETs mobility is more or less identical to that of SOI MOSFET's (Fig.4), indicating a real single crystal channel region achieved by this method. The single-grain nature of the active area can also be verified by the suppressed GIDL current as shown in Fig.5. This results in very high on-off current ratio for the LPSOI MOSFET.

The scaling property of threshold voltage is shown in Fig.6. LPSOI MOSFETs present a very good scaling abilities, in contrast to that of multi-grain conventional polysilicon TFT's, which show much more serious roll-off due to short-channel effects and grain boundaries variation. Device performance uniformity is another important factor for consideration. Unlike conventional TFTs which exhibit a serious performance variation introduced by the random distribution of grains in channel region, the LPSOI MOSFET exhibits much better uniformity due to its single-grain nature of channel region as shown in Fig.7 and Fig.8. This result shows that the LPSOI technology indeed SOI compatible and can be used to form high performance transistors on arbitrary insulators.

## 4. Conclusion:

The performance submicron LPSOI MOSFET fabricated by a high temperature annealed MILC is studied. The device performance for both n-channel and p-channel LPSOI MOSFET is similar to SOI MOSFETs. The process has also been shown to be highly controllable and resulting in devices with high uniformity.

## Acknowledgments:

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## Reference:

[1]. H. Kurino, et al. 1999 IEDM. p.879
[2]. S. Jagar, et al , *1999 Int'l SOI Conference*, p112.
[3].V. Subramanian, et al, *TED*, p1934, 1998.

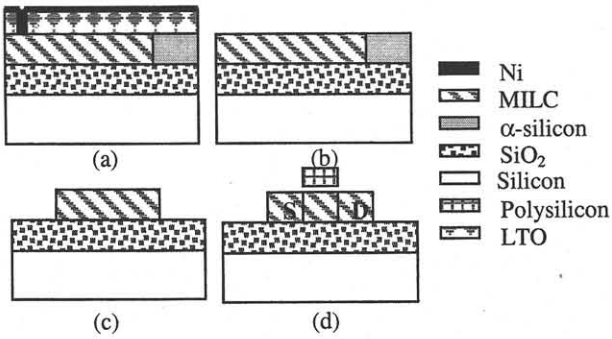


Fig. 1.Key steps for the formation of large grain poly-Si and LPSOI MOSFET fabrication.

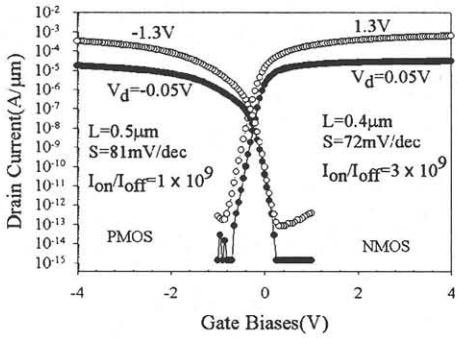


Fig.2. Subthreshold characteristics of n-channel and p- channel LPSOI MOSFETs.

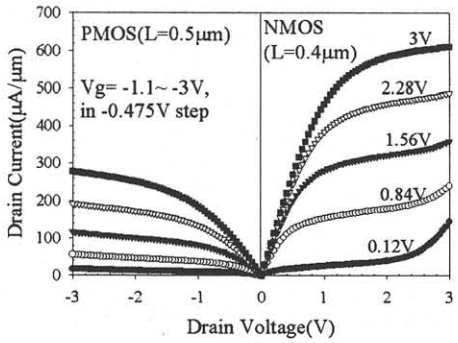


Fig.3. $I_d$-$V_d$ of LPSOI NMOSFET and PMOSFET

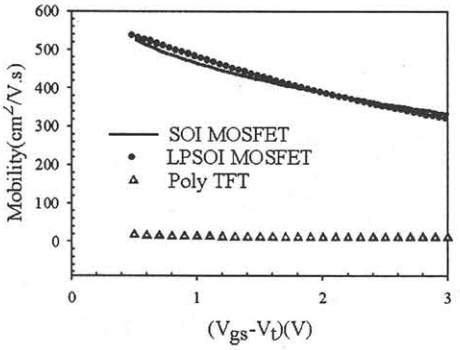


Fig.4. Mobility vs. $V_g$-$V_t$ of a SOI MOSFET, LPSOI MOSFET and a polysilicon TFT at $V_{ds}$=0.05V

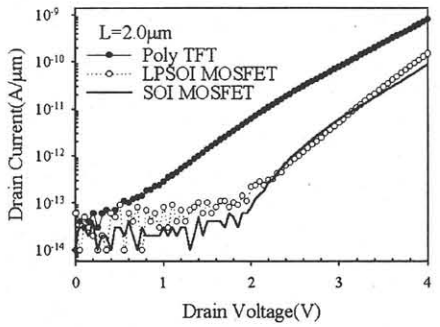


Fig.5. GIDL characteristics for a poly TFT, LPSOI MOSFET and a SOI MOSFET

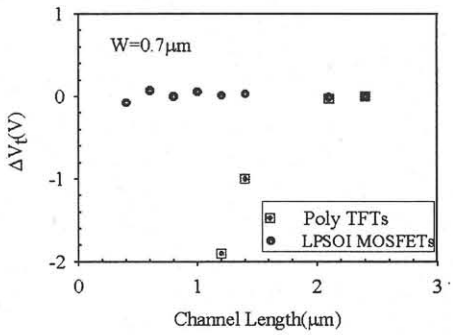


Fig.6. $V_t$ roll-off of LPSOI MOSFET and poly TFTs

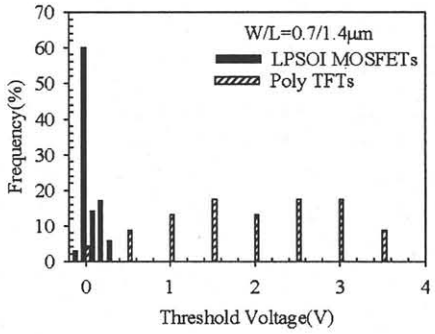


Fig.7. Uniformity of the threshold voltage across a wafer for poly TFTs and LPSOI MOSFETs

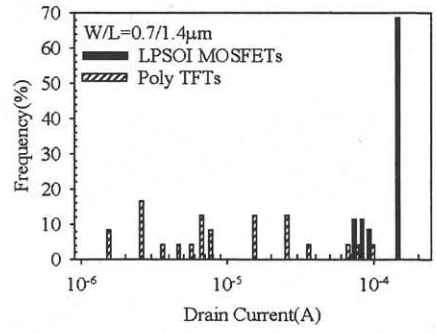


Fig.8. Distribution of $I_D$ ($V_d$=2V, $V_g$=3V) across a wafer for poly TFTs and LPSOI MOSFETs