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LE-2-3

Investigation on Reliability of High Quality Ultra-Thin ISSG Oxides

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1. Introduction

With continually aggressive scaling of devices, the direct tunneling gate leakage, boron penetration, and gate dielectric reliability have become increasingly important issues. Especially, the non-linear scaling of the power supply with the gate oxide thickness has imposed stringent restriction on the reliability as a result of the significantly increased electric field across the gate oxide [1]. It has been reported that, for ultra-thin gate oxides (<50Å), the oxide breakdown is controlled by the quality of the structural transition layer (STL) near the SiO_2/Si interface [2]. In this paper, we presented experimental results showing that ISSG oxides are much more robust than the dry furnace oxides. We believe that H_2 plays a vital role in improving the quality of the STL by reducing structural defects, such as weak Si-Si bonds and strained Si-O bonds.

2. Device Fabrication

NMOS and PMOS capacitors were fabricated on 200nm Si <100> wafers. 4 different thicknesses(36,22,18,15Å) of ultra-thin dry and 3 types of in-situ steam generated (ISSG) oxides were processed using diluted O_2 in a furnace and using mixed O_2/(1%)H_2 (standard ISSG), N_2/O_2/(1%)H_2 (dilute ISSG) or N_2O/(1%)H_2 (N_2O ISSG) in a clustered RTCVD chamber, respectively. Gases were directly introduced to the chamber without pre-combustion and the gas reaction occurs on the wafer surface. P/As and B were implanted on 2500Å poly Si gate respectively for NMOS and PMOS, followed by RTA N_2 anneal at 1000°C. The equivalent oxide thickness, EOT, was determined from high frequency (100kHz) C-V measurements considering the quantum-mechanical effect [3]. The area of tested devices is $5x10^{-5}$ cm^2 and reliability tests were carried out using the constant voltage stress (CVS) at 105°C.

3. Results and Discussion

Fig. 1 shows current densities at |Vg|=1.5V (Jg) versus EOT of furnace and 3 types of ISSG oxides for both NMOS (Fig. 1(a)) and PMOS (Fig. 1(b)). It can be clearly seen that, at a specified EOT, ISSG oxides exhibit lower Jg compared to furnace oxides. The higher presence of Hydrogen in the ISSG process, is believed to be responsible for the growth of better quality oxides.

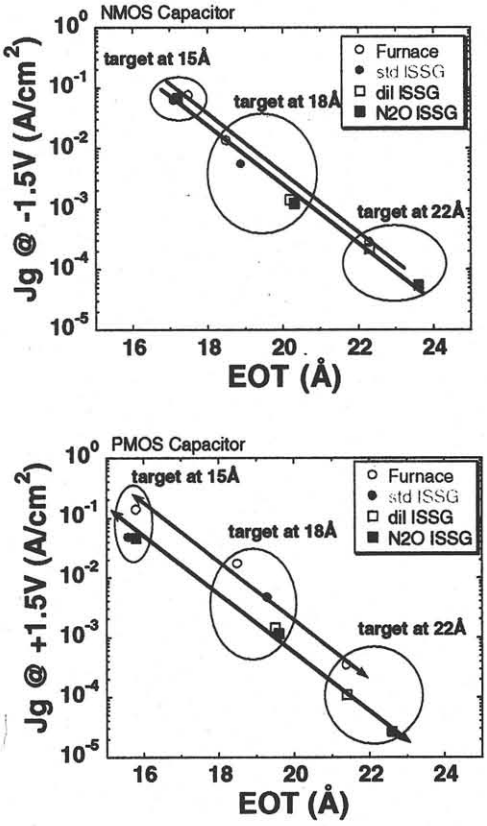

Fig. 1 Jg - EOT plots (a) NMOS; (b) PMOS

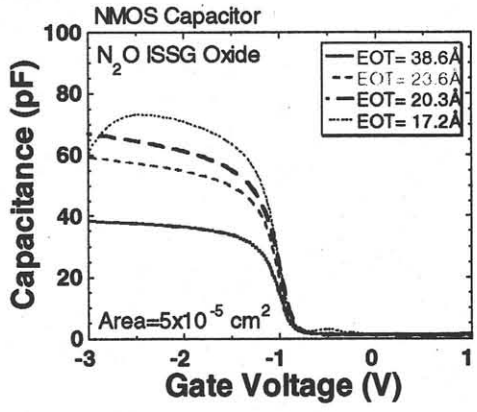

Fig. 2 C-V curves of different oxide thicknesses (N_2O ISSG oxide, NMOS)

The impact of this phenomenon on the quality of ISSG oxides will be discussed later. **Fig. 2** shows C-V curves of

different thicknesses of N_2O ISSG oxide. The slight difference in flat-band voltages(V_{FB}) indicates that the films have negligible fixed charges. Similar results are also found for the other oxides, as schematically illustrated in **Fig. 3**. Data of NMOS devices are linked by dotted lines while those of PMOS devices by solid lines. It is worthy to note that a significant positive shift of V_{FB} of various oxides is observed at 15Å target thickness. This could be related to a higher boron penetration. To investigate the quality of the SiO_2/Si interface and its influence on the oxide reliability, quasi-state and high frequency C-V measurements were conducted on thicker oxides. Comparable and low interface state densities (Dit) are shown between furnace, standard ISSG, and dilute ISSG oxides ($2\text{-}4x10^{10}$) whereas N_2O ISSG oxides exhibits lowest Dit ($\sim 3x10^9$), as shown in **Fig. 4**. To inspect the oxide quality, the charge-to-breakdown (Q_{BD}) at 63.2% from Weibull plots is used as an indicator. In addition, it has been reported that the ultra-thin (<50Å) oxide breakdown is dictated by the electron energy at the anode, which is determined by the applied gate voltage [4-6], so all reliability tests were performed using CVS. **Fig. 5** shows that all ISSG oxides exhibit larger Q_{BD} than dry oxides, and slight difference in Q_{BD} between ISSG oxides, implying that improved reliability is primarily contributed from the bulk instead of the SiO_2/Si interface. This conclusion is consistent with the report in [6]. The enhanced reliability of ISSG oxides may be explained by the fact that most of the defects, such as weak Si-Si bonds (O vacancies) and strained Si-O bonds, in the structural transition layer (STL) are significantly reduced due to generation of more reactive oxygen atoms as a result of the presence of H_2 during oxidation [7,8]. **Fig. 6** shows similar results from PMOS devices.

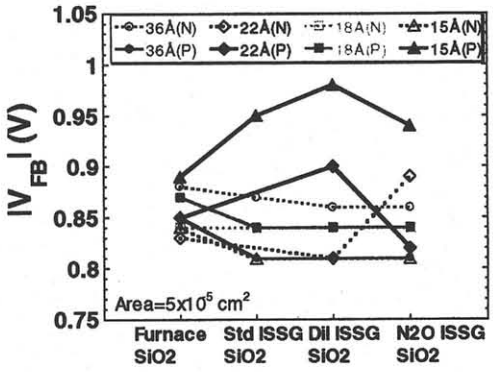

Fig. 3 V_{FB} comparison between different oxides and thicknesses

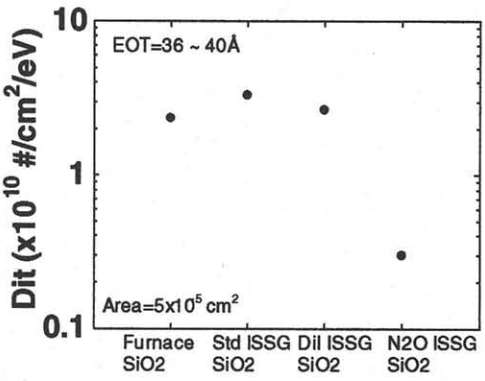

Fig. 4 Interface state densities (Dit) of different oxides

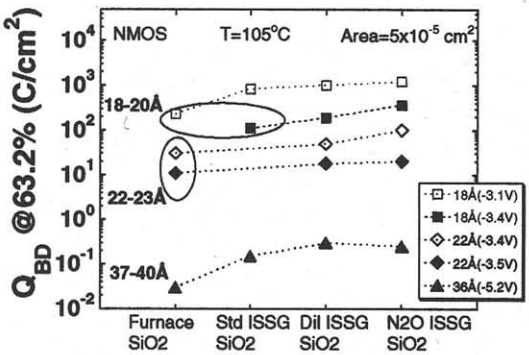

Fig. 5 Q_{BD}@63.2% comparison between different oxides and thicknesses (NMOS)

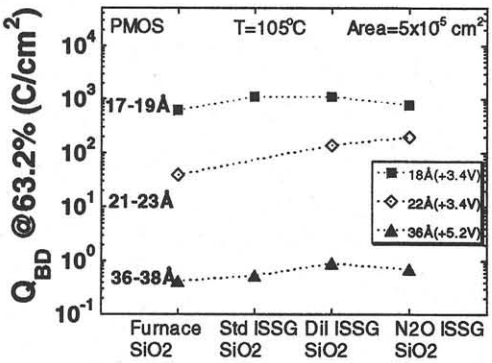

Fig. 6 Q_{BD}@63.2% comparison between different oxides and thicknesses (PMOS)

Conclusions

We have demonstrated the improved reliability of various ISSG oxides with EOT down to 18-20Å for both NMOS and PMOS, compared to the dry oxide. The better reliability of ISSG oxides is mainly due to the improvement in the bulk, instead of the SiO_2/Si interface. The presence of H_2 during oxidation is found to accelerate the oxide growth rate and enhance reliability of oxides by repairing defects in the STL.

References

[1] Y. Taur, et al., 1997 IEDM, p 215-218. [2] K. Eriguchi, et al., 1998 IEDM, p 175-178. [3] S.H. Lo, et al., IBM Journal of R&D, vol. 43, no. 3, p.327-338, May 1999. [4] T. Nigam, et al., 1998 IRPS, p.62-69. [5] E.Y. Wu, et al., 1999 IRPS, p.57-65. [6] P.E. Nicollian, et al., 2000 IRPS, p.7-15. [7] T. Hori, 1997 "Gate Dielectrics and MOS ULSIs", p.159-163. [8] T.Y. Luo et al., to be published in IEEE EDL, September 2000.