Extended Abstracts of the 2000 International Conference on Solid State Devices and Materials, Sendai, 2000, pp. 554–555

LE-2-6

Sub-2nm Equivalent SiO_2 Thickness Ta_2O_5 for Gate Dielectric Using RTA+UV/O_3

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1. Introduction

MOSFET dimensions are scaled down to obtain high speed, lower voltage and high density circuits. In the sub-0.1um gate length generation, ultra-thin SiO_2 is required to satisfy the scaling rule. However, since ultra-thin SiO_2 has high leakage current, we have to develop high-k insulator for gate dielectric.

Chemical vapor deposited Ta_2O_5 film is one of the most promising candidates for high-k gate dielectric[1]. We consider that Ta_2O_5 film has to meet two conditions to be used as gate dielectric. Firstly, Ta_2O_5 has high dielectric constant in crystalline state[2]. Ta_2O_5 after deposition is amorphous and we have to crystallize Ta_2O_5 with annealing. Secondly, since crystalline Ta_2O_5 has many O-vacancies which work as leak passes[3], oxidation process is needed.

Though rapid thermal oxidation (RTO) process satisfies these two condition, this method has the limit for obtaining thin equivalent SiO_2 thickness(Teq). Fig.1 shows Teq dependence on RTO temperature for 7.2nm physical thickness Ta_2O_5. The thinnest Teq was obtained at 800℃. Fig.2 shows XRD spectra of the samples shown in Fig.1. It was observed that crystallization occurred at 800℃. These two results confirmed that crystallization increased dielectric constant and implied that RTO grew SiO_2 in Ta_2O_5/Si interface and increased Teq at over 800℃. It was considered that RTO caused SiO_2 growth in Ta_2O_5/Si interface at around 800℃ and thinner Teq should be obtained by another annealing method without SiO_2 growth. We intended to break through this problem and obtain thin Teq using RTA+ultraviolet O_3 oxidation (UV/O_3). The schematic illustration of RTO and RTA+UV/O_3 are shown in Fig.3. Our new method crystallizes Ta_2O_5 with RTA and oxidizes Ta_2O_5 with UV/O_3. There are no SiO_2 growth during RTA without oxygen. Compared to RTO, UV/O_3 reduces SiO_2 growth because O-radicals are capable to oxidize Ta_2O_5 at lower temperature than by RTO and oxidation rate of Si is lowered with lower temperature.

2. Experiment

Fig.4 shows the process flow. We use p-type Si(100) wafer for the substrate. After cleaning the wafer with HF solution, SiO_2 layer was fabricated on the substrate to stabilize Si surface. From the point of view that Teq should be as thin as possible, chemical oxide was grown by hot solution ($HCl + H_2O_2 + H_2O$). Ta_2O_5 layer with 5-11nm thickness was deposited on SiO_2 layer by LPCVD using $Ta(OC_2H_5)_5$ and O_2 at 480℃. The thickness of Ta_2O_5 was measured by ellipsometry (the index=2[4]). After depositing Ta_2O_5, crystallization of Ta_2O_5 was done by RTA in Ar gases at 800C for 30sec. For reference sample, we crystallized Ta_2O_5 with RTO at 800℃ for 30sec. Next we oxidized Ta_2O_5 annealed by RTA using UV/O_3. MIS diodes were fabricated using Pt sputtering on Ta_2O_5. The diode pattern was 0.1mmΦ circle. Finally, sinter process was performed. For comparison, conventional 2.1nm Teq SiON reference diode was fabricated.

3. Results and Discussion

Firstly, we intended to optimize UV/O_3 conditon. The most important goal was to obtain thin Teq. It is considered that Teq becomes thick during UV/O_3 process because Si is oxidized by O-radical. For optimum UV/O_3 condition, no increase of Teq should be observed after UV/O_3 process. Fig.5 shows Teq at various UV/O_3 temperatures for 10.5nm physical thickness Ta_2O_5. UV/O_3 time was 2 minutes. Teq after UV/O_3 at the temperature from 150℃ to 350℃ was 2.5nm and it was clearly superior to that gained after RTO (3.3nm). It is concluded that UV/O_3 at the temperature from 150℃ to 350℃ suppressed SiO_2 growth in Ta_2O_5/Si interface and RTO promoted 0.8nm SiO_2 growth in Ta_2O_5/Si interface. Secondly, we determined the optimum condition for the leakage current. Fig.6 shows the leakage currents of the samples shown in Fig. 5 at the temperature from 150℃ to 350℃ which were the optimum conditions for Teq. The leakage current tended to be lower as temperature became higher, which showed that the optimum UV/O_3 condition was 350℃ and 2 minutes for 10.5nm physical thickness Ta_2O_5.

Fig. 7 shows Teq at various Ta_2O_5 physical thickness. In the case of RTO, Teq in the thin region (Ta_2O_5 physical thickness was around 6nm) was almost same as Teq in the thick region (Ta_2O_5 physical thickness was around 10nm). This is because O_2 reached to Si substrate as Ta_2O_5 became thin and SiO_2 growth was promoted and dominant at the same oxidation condition. The same effect occurred in UV/O_3 process. In the case that UV/O_3 temperature was 350℃, the change of Teq in the thin region was not large compared to Teq in the thick region. We avoided this problem with reducing UV/O_3 temperature from 350℃ to 300℃ to turn down oxidation power. As a result, Teq became thinner at 300℃ than at 350℃ in the thin region. As shown by the Teq line in Fig.7, the limitation of RTO process was broken through using RTA+UV/O_3. Finally, sub-2nm Teq was obtained in 5.3nm Ta_2O_5 physical thickness.

Fig. 8 shows the leakage currents of Ta_2O_5 and SiON. Teq of Ta_2O_5 was 2nm and that of SiON was 2.1nm. Leakage current of Ta_2O_5 was 2-orders of magnitude lower than that of almost the same Teq SiON.

4. Conclusion

We broke through the limit of RTO process using RTA +UV/O_3 method to anneal Ta_2O_5 gate dielectric. We realized sub-2nm Teq Ta_2O_5 as making Ta_2O_5 thin and controling UV/O_3 condition. We showed the superiority of leakage current of Ta_2O_5 compared to almost the same Teq SiON. Ta_2O_5 with 2nm Teq had 2-orders of magnitude lower leakage current than SiON with 2.1nm Teq.

References

[1]. Y. Momiyama et al., VLSI Tech. Dig. 135 (1997).
[2]. A. Chatterjee et al., IEDM Tech. Dig. 777 (1998).
[3]. J. V. Grahn et al., J. Appl. Phys. 84, 1632 (1998).
[4]. H. Shinriki et al., J. Electrochem. Soc. 145, 9 (1998).

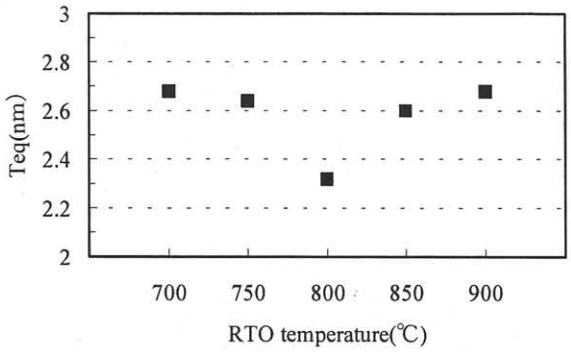

Fig. 1 Teq dependence on RTO temperature for 7.2nm physical thickness Ta2O5.

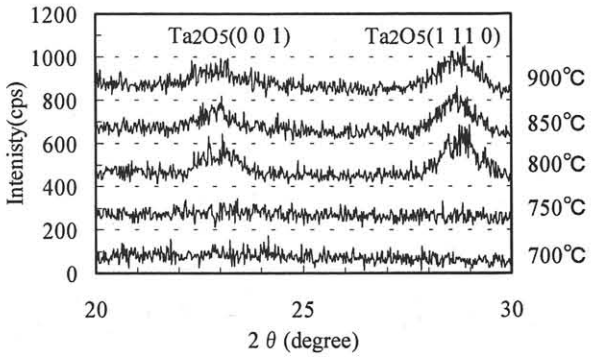

Fig.2 XRD spectra of Ta2O5 at various annealing temperatures.

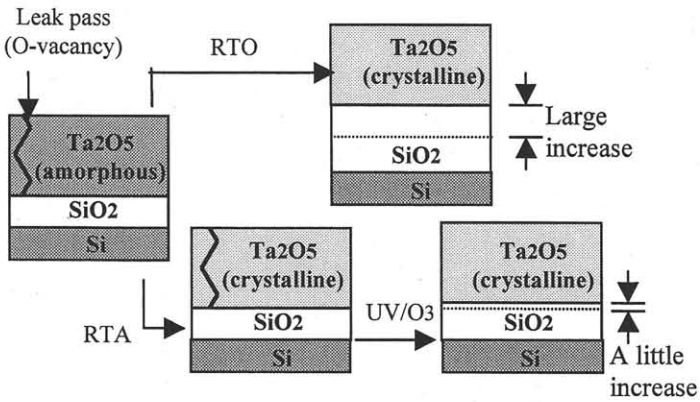

Fig.3 Schematic illustration of RTO and RTA+UV/O3.

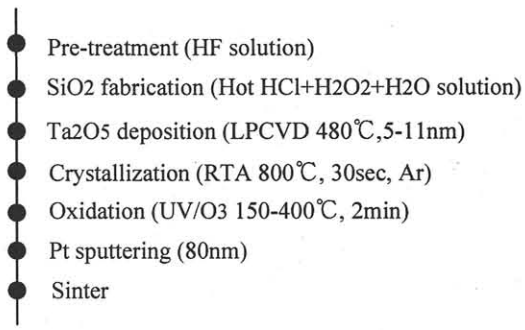

Fig. 4 Process flow.

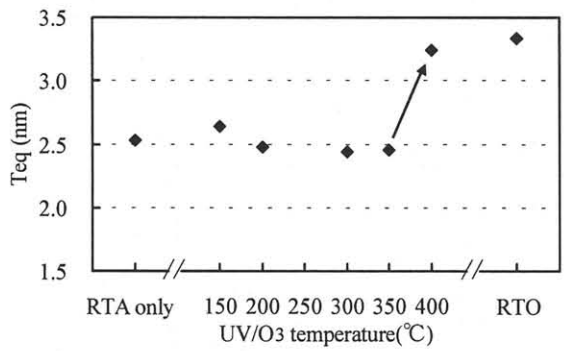

Fig.5 Teq at various UV/O3 temperatures.

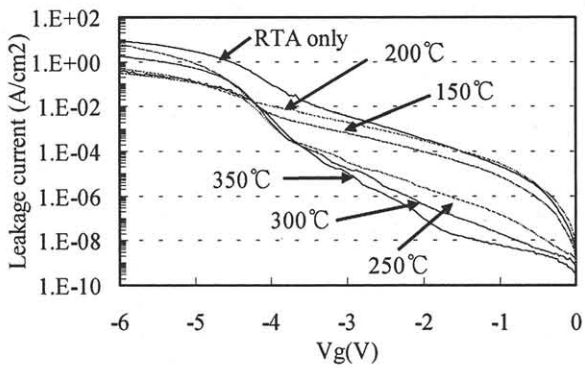

Fig.6 Leakage current at various UV/O3 temperatures.

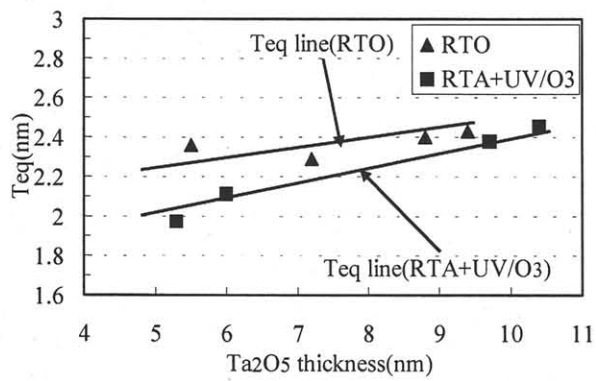

Fig. 7 Ta2O5 physical thickness and Teq.

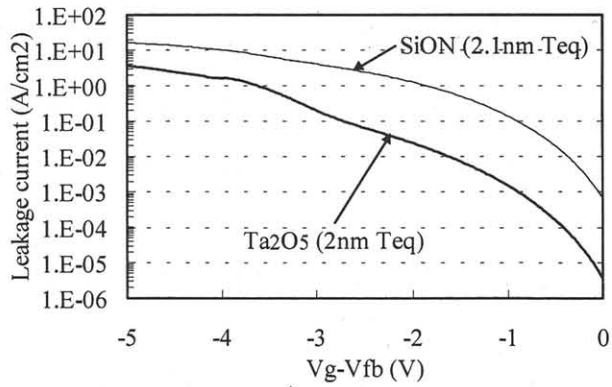

Fig.8 Leakage current of 2 kinds of gate dielectric (2nm Teq Ta2O5 and 2.1nm Teq SiON).