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P-2 (Plenary)

SOP and SOC: the Best of Both

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Introduction

Microelectronics technology, since the invention of the transistor, has revolutionized every aspect of electronic products in automotive, consumer, computer, telecommunications, aerospace, military, and medical industries by ever-higher integration of transistors at ever-lower cost per transistor. This integration and cost path has led the microelectronics industry to believe that this kind of progress can go on forever, leading to a so-called System-on-a-Chip (SOC) for all applications with all the system functions. The SOC is fast becoming the accepted norm and every company is working on it. It is becoming clear, however, that the SOC beyond the year 2007 presents major technical, financial, business, and legal challenges forcing industry and academic researchers to consider other options.

On the other hand, microelectronics packaging is going through paradigm changes of its' own. Contrary to the past, these changes are leading to thin, light portable and low cost technologies based on mixed- signal design and test, microvia board, integral passives, embedded optical waveguides, area array assembly, high heat flux3/4all based on large area intelligent manufacturing technologies, among others.

The intersection of these IC and packaging crossroads is paving the way for a fundamentally new paradigm that is referred to here as SOP, System-on Package. Thus, SOP brings the best combination of IC and packaging technologies for continued microelectronics growth.

Fundamental Limits in SOC Technologies

The single most important emerging fundamental problem seems to be the so-called "latency" in the IC interconnect rise time. For example, the switching speed and the rise time at 1 micron-level technology are 10 picoseconds and 1 picosecond respectively. However, these numbers at .05 micron-level deteriorate dramatically to a level that while the switching speed improves from 10 PS to 1 PS, it is the interconnect rise time that dramatically slows down to about 100 PS, as indicated in Table 1.

The other fundamental problem seems to be the absence of insulating property of SiO2 dielectric as the dielectric thickness is scaled down to five molecular thicknesses. These are major problems that the industry will face as it develops IC lithography to these dimensions.

Table 1: Fundamental Limits

Technology Generation	MOFSET Intrinsic Switching Delay	Response Time*
1.0μm	~10 ps	~ 1 ps
.05 μm	~1 ps	~100 ps

*L_{INT}= 1mm

Table 2: Fundamental Giga-scale Issues

FUNDAMENTAL TECHNICAL:
- IC Signal Speed "Latency"
- SiO_2 Dielectric Insulation

ENGINEERING:
- Mixed Function Costs
  - $30/cm² µP, DSP
  - $15/cm² FPGA
  - $10/cm² DRAM
  - $5/cm² Analog
- Electrical Costs
- Lower Yields: .07µ litho, on 3.5 cm & IC from 400 mm wafer
- Extra Mask Steps, Phase Shift @197 nm

FINANCIAL:
- $5B Plant

LEGAL:
- IP Integration Wars

Engineering and Financial Limits of SOC Technology

In addition to fundamental limits, integration of multiple functions onto SOC is expected to result in engineering issues as well as financial and investment issues in setting up wafer fabs that could cost as much as $3 to $5B, as indicated in Table 2.

System-Level Packaging

The most important solution is to keep the interconnect short. However, this will not be easy when the on-chip interconnect is projected to be almost 5000 meters in length compared with 50 meters at 1 micron-level. The other option is to use multichip-packaging technologies where the global interconnect is provided by the on-package wiring. While this is a potential solution to the IC interconnect latency, it does not offer a total system solution. Any system-level solution has not only to provide high-speed digital but also high-bandwidth optical, analog, RF and perhaps MEMS. This is more than an MCM (as it has existed in the past).

System-Level Packaging Evolution

A system-level view of packaging to date is illustrated in Figure 1. It includes not only IC packaging but also system-level board packaging including discrete and other components. While this evolution has led to improved component density, it has not met the cost needs for consumer products. In contrast to

Figure 1: Packaging Evolution

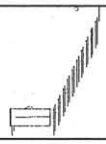
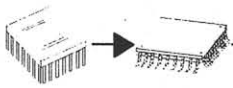
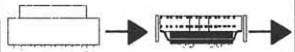
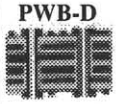
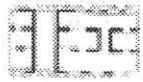
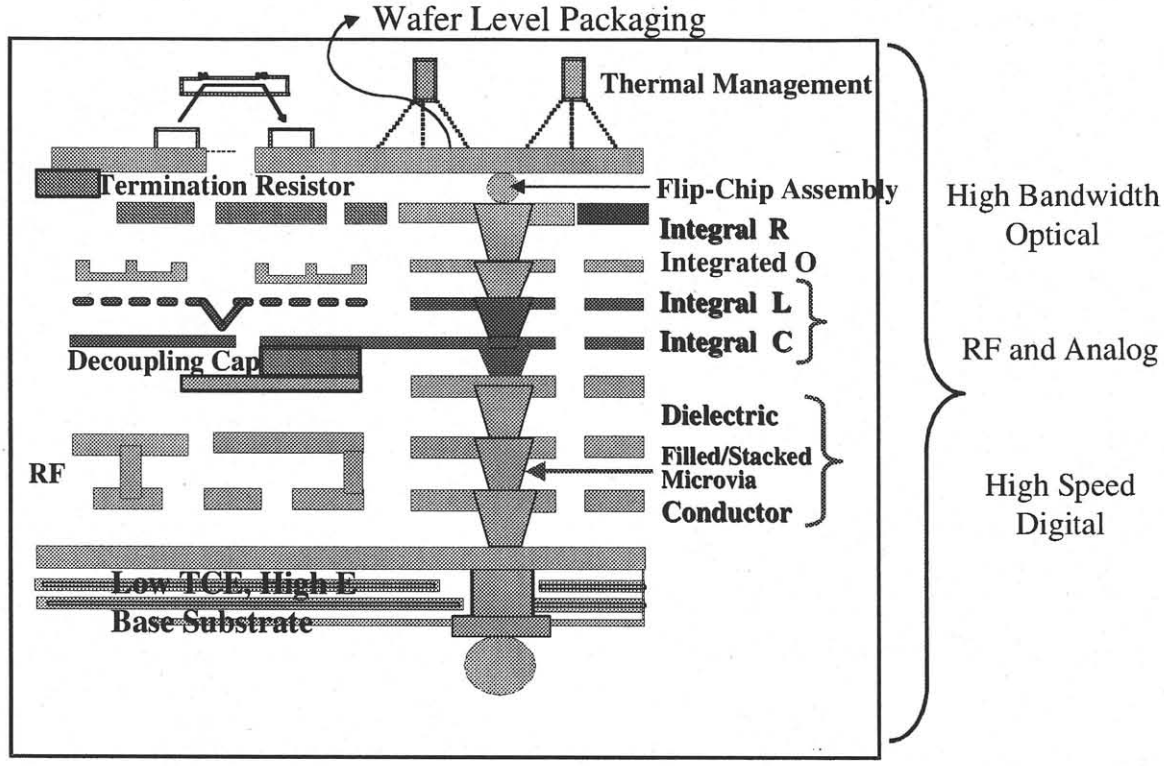
	1970's	*1980's*		*1990's*		*Next Need*	
	DIP	**PGA**	**QFP**	**BGA**	**CSP**	**Wafer-Level Packaging with SOC/SOP**	
Single Chip:						?	• *High-Speed Digital*
Chip Connector:	Wirebond	Redistribution to Area Array		Flipchip Area Array			• *High Band-Width Optical*
Board MCM:	Ceramic	Ceramic or Thin Film on Ceramic		Thin Film on PWB			• *RF*
Board:	**PWB-D** 	**PWB-D** 		**PWB-Micro Via** 			• *Analog*
Board Connector:	PTH	Peripheral SMT		Area/BGA SMT			• *MEMS*
Discretes:	**1005**	**0805 → 0603**		**0402**		**0201**	

Figure 2: Cross-Section of a Single-Level Integrated Module (SLIM)



the cost of all ICs used in a system, the cost of packaging at system-level for most applications has been high. This is leading the industry to believe that on-chip integration is a better strategic direction. This of course is leading to the SOC strategy.

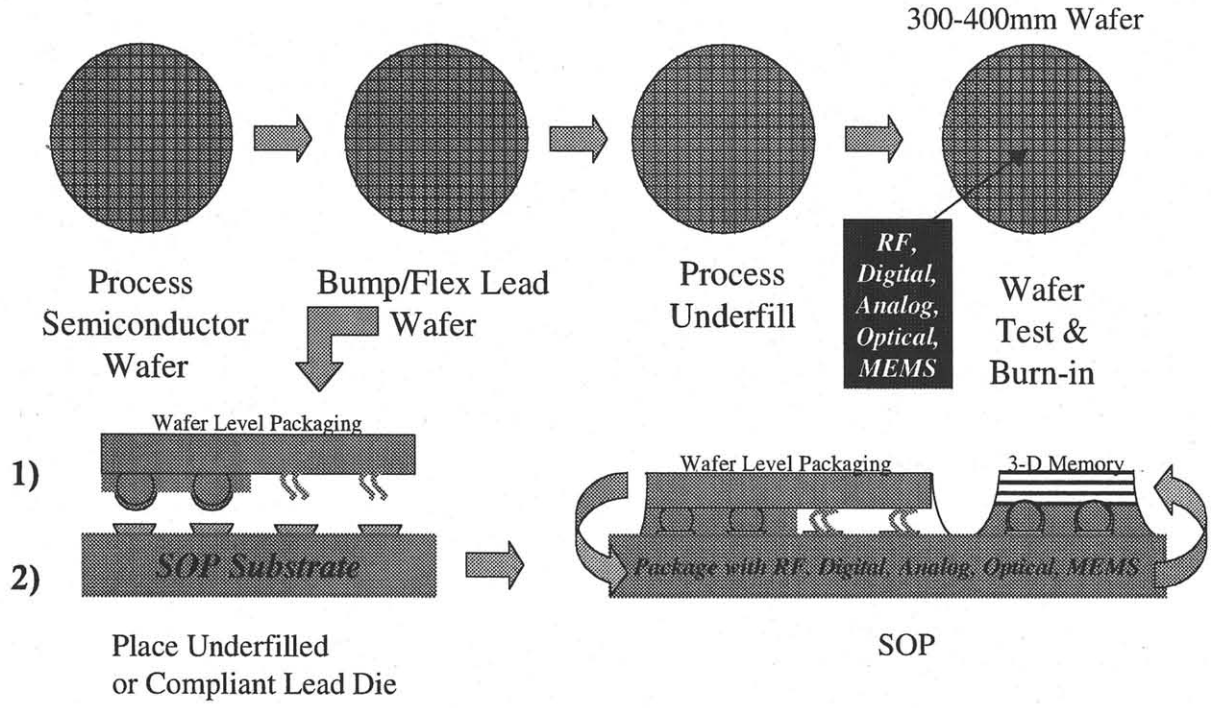
However, a team of several universities and a number of companies under the leadership of the Packaging Research Center at Georgia Tech funded by NSF-ERC have been working on a fundamentally new paradigm called System-on-Package. SOP seems to provide technical, financial, legal and business solutions to the system-level problems for three classes of systems: (1) network servers, (2) wireless base stations and handsets and (3) optical network systems for interactive videos. The SOP technology involves integration of high-speed digital wiring by means of ultra high-density copper global interconnect in ultra low-dielectric constant polymer material, high-bandwidth optical by means of optical waveguides buried in the package and analog and RF functions by means of buried integral passives. The MEMS functions are similarly incorporated as well into the package. This is referred to as SLIM packaging, or Single-level Integrated Module. A cross section of SLIM indicating various functions is illustrated in Figure 2.

The SOP concept thus includes two components (Figure 3): 1) highly integrated packaging like SLIM and 2) next-generation IC technologies such as wafer-level packaging with burn-in and test (as being pursued by Professor Meindl at Georgia Tech). SOP thus requires major enhancements in IC Technologies and integrated packaging technologies. In addition to the largest IC that can be economically fabricated with the required digital, analog, RF and optical functions, the ICs will be fabricated with wafer-level burn-in, electrical test and flexible I/O connections. This is referred to as wafer-level packaging.

SOP Accomplishments

A number of accomplishments have already been made, demonstrating the feasibility of the SOP concept. These accomplishments include demonstration of integral capacitors, resistors and inductors as well as high-density global interconnect, new mixed-signal design, low cost electrical test, among others.

Figure 3: Two Components of System-On-a-Package (SOP)



The PRC's mixed-signal test group recently broke new ground in the testing of complex analog ASICs. The newly developed test technique allows an order of magnitude speed-up over current specification-driven production test methods in test application time, while significantly reducing the complexity of test instrumentation and production tester load boards. All of this is achieved without compromising the coverage of the applied tests.

The technique rests on the principle of generating a transient test stimulus such that the response of the circuit under test is sensitive to any silicon process perturbations that also affect the circuits' specifications. Hence, the original specification-driven tests can be replaced by the fast transient method during production testing. Further, it is possible to compute the circuits' specifications with a high degree of accuracy from the transient test response itself. The computed specification values are then subjected to modified thresholds for pass/fail acceptance. Validation of the technique has been performed with the support of National Semiconductor Corporation on one of their high-speed opamps.

The high density wiring thrust has demonstrated the ability to rapidly cure polymer thin film dielectric materials. Commercial dielectric materials often require many hours of thermal processing (e.g. three to six) in order to achieve fully processed material. The thermal treatment is required to carry out the chemical reactions, remove reaction products, and (at times) achieve a particular stress level. Variable frequency microwave and electron beam-induced curing was shown to produce equivalent materials in only a fraction of the time-typically less than 20 minutes in comparison to three to six hours. This is the first demonstration of curing HD 2611 polyimide to produce a low-stress, cured polymer in 20 minutes. The rapid ramp rate and method of energy transfer are thought to be responsible for the low stress state.

Flipchip microelectronic packaging, the technology of attaching semiconductor chips directly to circuit cards, is experiencing rapid growth driven by the demand for faster, smaller, and more reliable electronic systems. However, costly manufacturing processes and materials, as well as inadequate manufacturing infrastructure, have hindered wide-scale proliferation of flipchip technology to date. The PRC team has jointly created next-generation flipchip manufacturing processes, advanced materials, and manufacturing equipment with the potential to achieve up to 2-6 times cost savings over traditional flipchip approaches.

Via formation is a critical process sequence in multi-chip-module and SOP technology, as it greatly impacts yield, density and reliability. Modeling, optimization and control of via formation are crucial in order to achieve low-cost manufacturing. The PRC's Intelligent Large-Area Manufacturing thrust team has developed a model-based supervisory control algorithm and applied this algorithm to reduce undesirable behavior resulting from various disturbances in the via formation process. A series of designed experiments were used to characterize the via formation work-cell (which consists of the spin-coat, soft-bake, expose, develop, cure and plasma de-scum unit process steps). The output characteristics considered were film thickness, uniformity, film retention and via yield.

Recently, regulatory pressures-particularly from Japan and Europe-to eliminate lead-containing solders from electronics packaging have increased. The increased Center membership of companies from these countries prompted the PRC to add an environmental focus to its research programs, thus shifting to a more systematic approach to its "System-on-a-Package" technologies. One of these research areas focuses on alternatives to tin/lead solders by means of electrically conductive adhesives (ECAs). However, for several years the unstable resistance and poor impact-strength of current ECAs have been the bottleneck for incorporation of this new technology into products. The PRC team made a ground- breaking discovery pointing out for the first time that galvanic corrosion is the main mechanism behind the unstable contact resistance. This important finding won Mr. Lu the 8th Motorola-IEEE/CPMT Graduate Fellowship for Research in Electronics Packaging at the 49th ECTC in 1999. The Georgia Tech team also discovered a few ingredients able to stabilize the ECA resistance and the team have synthesized a few epoxy resins showing superior impact strength.

The trends in IC technology such as reduced feature sizes, increased I/O and enhanced performance are imposing stringent requirements on wiring substrates. Conventional PWBs are unable to meet the wiring density needs to provide interconnections of advanced ICs. To meet these needs, the industry has come up with several new so-called "microvia" technologies that allow fabrication of small vias and fine lines using existing processes that have been practiced for a decade on large-area boards. These technologies, while meeting today's needs, must be upgraded for the needs of tomorrow. The PRC team has begun working on entirely new approaches and have successfully demonstrated two novel processes for planar multi-layer, high-density, thin film wiring substrate fabrication. Both the plated-post photo-polymer (P4) process and the via-less process utilize the newly developed materials and large-area processes that have led to lower cost. The P4 process is characterized by via-post plating prior to thin film dielectric deposition and via hole opening on top of the via-post. This construction enables via filling and stacking without the expensive and complex planarization process step. The via-less process is a further simplification of the P4 process by a tight control of the height of the plated post and the elimination of the via hole opening process. Metallization is semi-additive with electroless seeding followed by electro-pattern plating, which enables fine-line patterning. These two processes have demonstrated a number of four-layer build-up of thin film wiring substrates. Superior surface planarity, micro-via filling and stacking and fine-line patterning are achieved. Key enabling factors are identified and the resulting structures are characterized for these two processes. The typical feature sizes evaluated are 100 mm via-post diameter, 20-25 mm via-post height, 50 mm via-hole diameter, 25 mm dielectric thickness, and 9 mm copper thickness.

The Georgia Tech PRC RF thrust has developed compact high-Q inductor and capacitor topologies and implemented in multi-layer ceramic-based MCM technology. The inductor architecture is based on the multi-level ground plane and helical configurations. The novel capacitor architecture is based on the vertically interdigitated topology which considerably reduces the area compared to the conventional parallel plate capacitor implementation. The optimized embedded inductors lend double the self-resonant frequency, triple the Q and occupy an order of magnitude area smaller than the conventional spiral inductors. Both three-dimensional L and C design concepts have been applied to the development of an embedded passive library whose components have been directly used in a 1.9 GHz DECT hybrid Si-MCM power amplifier. In addition, novel compact filters have also been developed using stacked, coupled stripline and double ground plane lumped-element architectures, which exploit the multi-layer capabilities of the technology and shrink the filter size that typically occupies the largest board real estate. Both filters are used in the front-end 2.4 GHz and 5.8 GHz wireless LAN transceiver systems.

Summary

In summary, a fundamentally new paradigm called System-on-Package could potentially become a

complementary alternative to System-on-Chip, thus providing a balanced set of system-level functions between the semiconductor IC and single component package beyond the year 2007. The concurrent engineering and optimization of IC and package could overcome the fundamental IC issues presented above.

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