Extended Abstracts of the 2001 International Conference on Solid State Devices and Materials, Tokyo, 2001, pp. 8–9

A-1-1 (Invited)

Recent Progress in High-k Dielectric Films for ULSIs

Sang In Lee
Semiconductor R&D Division, Samsung Electronics Co., Ltd.
San #24, Nongseo-Ri, Kiheung-Eup, Yongin-City, Kyunggi-Do, Korea, 449-711
Tel: 82-31-209-6318, Fax: 82-31-209-3319, e-mail: silee215@samsung.co.kr

1. Introduction

The ITRS specifies a rapid scaling of ULSI device in the next decade. The most important technology to scale the device is related to high-k dielectric which is capable of replacing SiO_2 on silicon for CMOS and Nitride/Oxide (NO) capacitor dielectric for DRAM. In this talk, few key questions and some plausible answers for gate dielectric of CMOS and capacitor one of DRAM will be described. Promising candidates of high-k dielectric as well as atomic layer deposition (ALD), most favorable technique for the growth of high-k dielectric films, will be introduced.

2. Requirements for High-k Gate Dielectric for CMOS

For a planer CMOS with 70nm node and beyonds, the gate dielectric EOT is required to be 8 - 12Å according to ITRS roadmap. The intensive research has been made on high-k and NO stack gate dielectric because the scaling limit of gate oxide (SiO_2) is believed to be 12Å by considering the gate tunneling leakage and DC performance degradation.[1] The general requirements for high-k gate dielectrics are listed in Table 1. First, dielectric constant over 15 and the thermal stability on silicon are desired. Second, the amorphous high-k dielectric is preferred because the polycrystalline high-k gate dielectric may lead to higher leakage current due to grain boundaries as current paths and a lattice mismatch with silicon. Third, a fixed charge generation resulting in flatband voltage (V_{fb}) shift should be disclosed.

3. Requirements for High-k Capacitor Dielectric for DRAM

A considerable attention has been paid to develop a storage capacitor for the next generation of conventional NO dielectric in order to satisfy sufficient cell capacitance. There are two major requirements for the high-k capacitor dielectric in terms of material properties. Large dielectric constant is favorable to provide sufficient capacitance in the limited capacitor area. Also, the leakage current through the dielectric must be low enough to prevent the refresh problems. Besides material properties, the deposition method of high-k dielectric film on the complicated three-dimensional structure is required to be available. The dielectric constant of high-k candidate oxides for capacitor integration are listed in Table 2.

4. Aluminum Oxide for CMOS and DRAM

Even though Al_2O_3 film is an attractive material as gate dielectric due to the excellent thermal stability with silicon[2], the application of Al_2O_3 film as gate dielectric suffered from the V_{fb} shift caused by fixed charge.[3] As shown in Fig. 1, the negative fixed charge in Al_2O_3 film induced not only V_{fb} shift but also degradation in the channel mobility of MOS transistor.

Recently, metal-insulator-silicon (MIS) capacitor integration has been applied into mass production based high density DRAM. Even though Ta_2O_5 film is a major high-k dielectric for the MIS capacitor integration, SiON film is required between Ta_2O_5 and storage poly Si node in order to prevent reaction. The technical trend of scaling for MIS Ta_2O_5 capacitor is the integration of metal-insulator-metal (MIM) Ta_2O_5, which requires Al_2O_3 encapsulating barrier layer for preventing hydrogen attack during ILD and alloy process.[4] As an alternative high-k dielectric, Al_2O_3 film has been suggested because of excellent insulating property and thermal stability on Si.[4, 5, 6] As shown in Fig. 2, fully working 1Gbit DRAMs with design-rule of 0.15 and 0.13μm were fabricated with SIS Al_2O_3 and MIS Al_2O_3 capacitors, respectively.

5. Doped Aluminum Oxide

The MIM Ta_2O_5 capacitor requires the changing of the storage node material from poly Si to metal, which suffers from the significant modification of full integration scheme of DRAM. Alternatively, the extendibility of MIS Al_2O_3 capacitor can be achieved by simple doping into Al_2O_3 film because it can improve insulating property as well as enhance dielectric constant. Simple modification of dielectric film does not require any change of integration scheme, unlikely to the case of Ta_2O_5 capacitor. Fig. 3 and Fig. 4 show the improved I-V characteristics of Ti and Hf doped Al_2O_3 capacitor, respectively. Additionally, it was reported that the Zr doped Al_2O_3 film has improved insulating property.[7]

For the high-k gate dielectric for CMOS technology, Hf doped Al_2O_3 film can be promising candidate because both drawbacks of HfO_2 and Al_2O_3, which are polycrystalline phase and fixed charge, respectively, can be suppressed. Moreover, demand for the further scaling will be potentially satisfied with higher dielectric constant which can be easily adjusted by increasing amount of dopant.

6. ALD Technique for High-k Dielectric Growth

ALD is known as the most adequate technique for thin film growth because of its nature of surface controlled process and has excellent characteristics of uniformity, step coverage, exquisite thickness control, stoichiometry, and delta-doping capability.[8] Ti, Hf, and Zr doped Al_2O_3 film can be deposited by using ALD. Also, SiN layer of NO stack gate dielectric requires atomic level thickness controllability, which can be accomplished by only ALD. Furthermore, the dielectric films with k over 100 such as $SrTiO_3$, $(Ba,Sr)TiO_3$, and $SrTiO_3/BaTiO_3$ nanolaminate may need to utilize the advantage of ALD technique. Fig. 5 shows TEM image of nanolaminate dielectrics grown by ALD technique.

7. Conclusion

Requirements and plausible solutions of high-k gate dielectric for CMOS and capacitor dielectric for DRAM were discussed. Hf or Ti doped Al_2O_3 film can be promising candidate in terms of thermal stability and compatibility with silicon. Most of promising high-k dielectrics can be grown by ALD, which is the most adequate technique of the thin film process for ULSIs.

Acknowledgments

The authors would like to thank IPS Co. in Korea and Genus in USA for their sincere support to the deposition of high-k films by using ALD technique.

References

[1]. B. Yu, et. al., Symp. on VLSI Tech., p. 9 (2001).
[2]. E. P. Gusev, et. al., Appl. Phys. Lett. 76, p.176 (2000).
[3]. J. H. Lee, et. al., IEDM, p. 645 (2000).
[4]. Y. K. Kim, et. al., IEDM, p. 369 (2000).
[5]. I. S. Park, *et. al.*, Symp. on VLSI Tech., p. 42 (2000).
[6]. Y. K. Kim, *et. al.*, Symp. on VLSI Tech., p. 52 (1998).
[7]. L. Manchanda, SSDM, p. 150 (1999).
[8]. Y. Kim, et. al., Appl. Phys. Lett. 71, p.3604 (1997).

Table 1. Requirements for high-k gate dielectrics.

Criteria	Target	Requirements
EOT	≤ 10Å	Dielectric Constant ≥ 15
LKG	< 1A/cm²	Bandgap Eg >5eV, CB Offset >1eV
Thermal Stability	No Reduction and No Silicidation	Si+MOx→M+SiO_2 ;△G>177kJ/mol 270(Al_2O_3)/200(HfO_2)/177(ZrO_2) Si+MOx→MSix+SiO_2 ;△G>0kJ/mol Higher Heat of Formation ; ∣△Hf∣ ≥ 911kJ/mol(SiO_2) 1676(Al_2O_3)/1134(HfO_2)/1096(ZrO_2)
△V_{fb}	< 10mV	Less Oxide Trap Charge
Dit	<10^{11}/eVcm²	Amorphous Phase (Interface with Si-sub.)
Mobility	> 90% of SiO_2	Less Fixed and Interface Trap Charge Less Metal Impurity in Si-substrate

Table 2. Dielectric constants of high k candidate dielectrics..

	SiO2	Al_2O_3	ZrO_2	HfO_2	Ta_2O_5	TiO_2	$SrTiO_3$	BST
Dielectric constant	3.9	10	20	22	25	60	100	>200

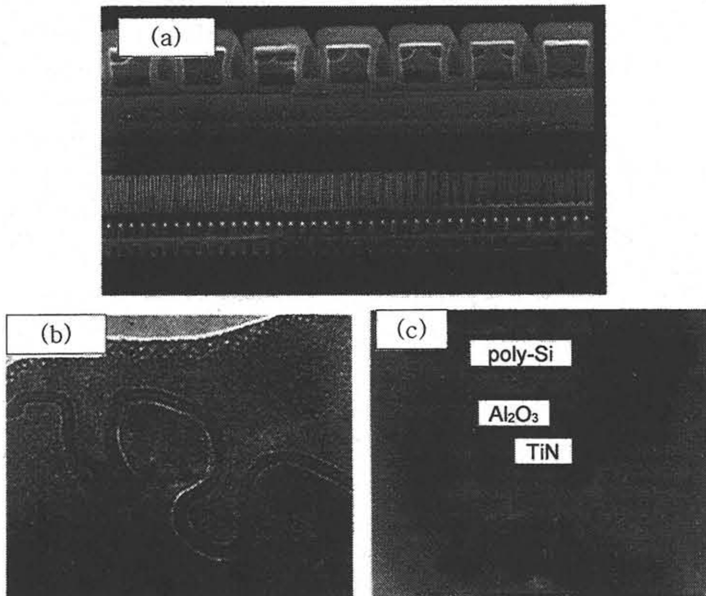

Fig. 2. (a) Cross sectional SEM micrograph of cell array in 0.13μm design rule based 1Gbit DRAM with Al_2O_3 capacitor. (b) TEM micrograph of applied SIS Al_2O_3 capacitor, (c) TEM micrograph of applied MIS Al_2O_3 capacitor.

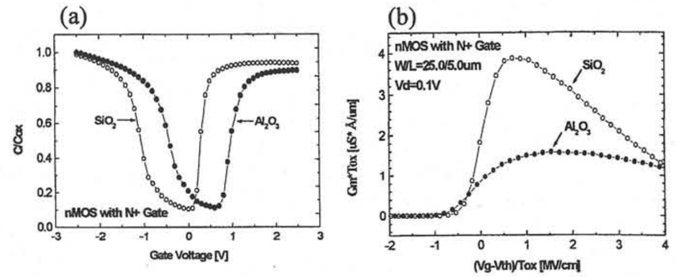

Fig. 1. Comparison of (a) C-V curves and (b) Normalized transcoductance (Gm) of nMOSFET with Al_2O_3 and SiO_2 gate dielectrics.

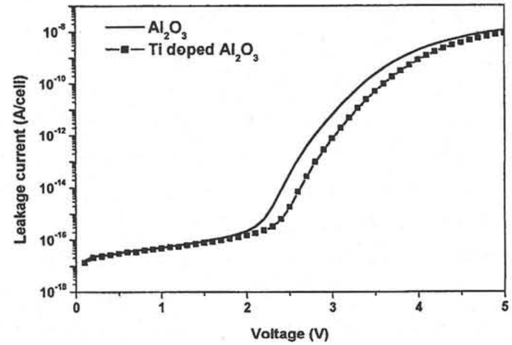

Fig. 3. Comparison of I-V characteristics of Al_2O_3 and Ti doped Al_2O_3 capacitor with identical EOT of 30Å.

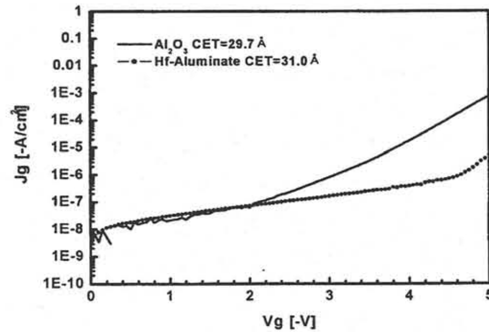

Fig. 4. Comparison of I-V characteristics of Al_2O_3 and Hf doped Al_2O_3 gate dielectrics.

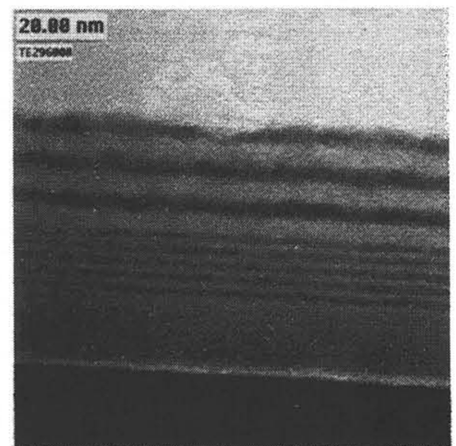

Fig. 5. TEM micrograph of nanolaminate dielectrics grown by ALD technique.