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Spin-Drying with CO₂ Gas Purge for 0.13 μ m DRAM's Contact Process

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1. Introduction

In semiconductor device manufacturing, wet cleaning process basically consists of chemical treatment, de-ionized water (DIW) rinsing and drying. For 300mm wafer, high performance and cost effective cleaning processes have been proposed. Also, DIW rinsing and drying processes after chemical treatment becomes more important, because the minimized device structure becomes more sensitive to static electricity induced during rinsing and drying processes. Then, we investigated the influence of static electricity on contact resistance between the bit line and silicon substrate in 0.13 μ m DRAM. In this paper, we made it clear that rinsing with CO₂ gas dissolving water and spin-drying with CO₂ gas purge were effective to prevent the semiconductor device from the static electricity during rinsing and drying.

2. Experiment

The sample structure to clear the influence of static electricity during rinsing and drying is shown in Fig.1. P doped poly-silicon was used as a plug material between the bit line and silicon substrate. Fig.2 shows the schematic diagram of single wafer cleaning system used in this study. This system has two chambers. 1st chamber (cham.1) performs a chemical etching and rinsing. 2nd chamber (cham.2) is for a final rinsing and spin-drying. The sequence of wafer treatment is shown in Table1. After RIE process of contact holes, the oxide on the bottom of holes was etched with BHF (3weight% HF and 39weight% NH₄F) for a few seconds at cham.1, immediately followed by water rinsing for 30 seconds at the same chamber. These wafers were then transferred to cham.2 without drying. These wafers were rinsed again and spin-dried. The rotation speed of the chemical treating and rinsing was 1000rpm and that of the drying was 2500rpm, respectively. The resistance of CO₂ gas dissolving water for rinsing was 0.01-0.1M Ω cm. We measured the contact resistance between bit line and silicon substrate with or without CO₂ dissolving water and CO₂ gas purge effect. We also observed the interface between poly-silicon and silicon by the cross section TEM.

3. Results and discussion

Fig.3 shows the results of the contact resistance. In case of DIW rinsing and spin-drying without CO₂ gas, 86% chips in 200mm wafer were found to be high resistance above 8K Ω . Especially, the center chip on the wafer had the highest contact resistance. Photo.1 shows the TEM result. It was found that silicon oxide was formed at the interface of poly-silicon plug and silicon substrate. It is clear that abnormal oxidation of silicon substrate caused the high contact resistance. Fig.4 shows the correlation between thickness of silicon oxide and rinsing time in center position. In case of DIW rinsing, it was found that thickness of silicon oxide increased with rinsing time. The DIW rinse nozzle was set forward the wafer center. The static electricity generated by the friction of rinse water and substrate or rinse water and air promoted the abnormal oxidation at wafer center during rinsing. On the other hand, in case of using of CO₂ gas dissolving water for rinsing instead of DIW, it was found that the silicon oxide was not formed in center position. Also, the contact resistance became lower to 3K Ω , as shown in the middle of Fig.3. However, contact resistance still has a wide variation. Fig.5-a shows a map of contact resistance in a wafer. The wide variation resulted from higher contact resistance of peripheral chips. Fig.6 shows the vapor pressure of CO₂ and H₂O. As CO₂ gas vaporizes from CO₂ gas dissolving water more easily than H₂O in drying step, it is supposed that static electricity generated again at wafer edge with large angle velocity during drying step. Therefore, CO₂ gas purging was carried out to prevent from the selective vaporization during spin-drying. The effect is shown in Fig.3 and Fig.5-b. The low contact resistance with uniform distribution was realized in 200mm wafer.

4. Conclusion

We could clear that abnormal oxidation during rinsing and drying caused the high contact resistance. We also succeeded in preventing the semiconductor device perfectly from the static electricity by using of rinsing with CO₂ gas dissolving water and drying with CO₂ gas purge. In single wafer cleaning system, the drying method with CO₂ gas purge is the important technology for future devices.

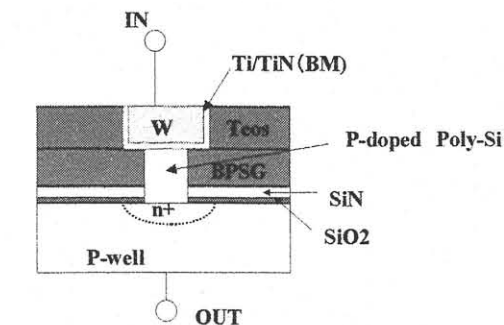


Fig.1 Sample structure

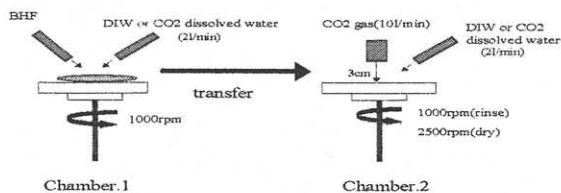


Fig2 Single wafer cleaning system

Table1 Treatment sequence

Step	sequence	cham.No	time(sec)	rotation speed(rpm)
1	BHF	1	10	1000
2	rinse	1	30	1000
3	rinse	2	N	1000
4	dry	2	60	2500

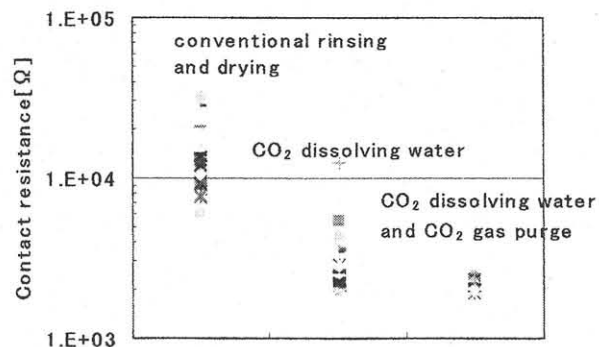


Fig.3 The variation of contact resistance by rinsing with CO₂ dissolving water and drying with CO₂ gas purge

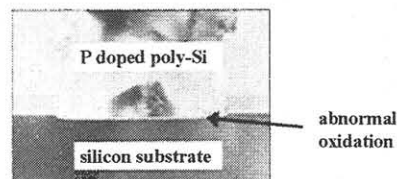


Photo.1 The cross section photograph (TEM) of bottom interface of contact hole.

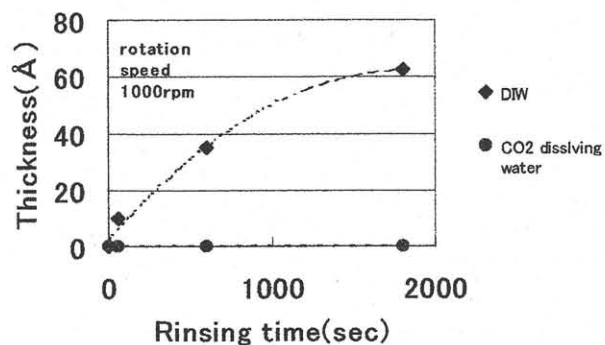


Fig.4 The correlation between thickness of silicon oxide and rinsing time in center position of wafer

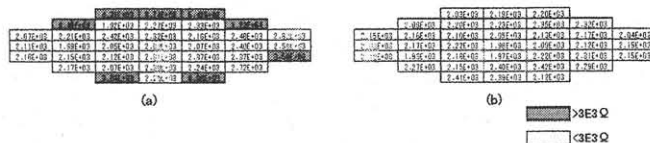


Fig.5 A map of contact resistance in a wafer (a) only rinsing with CO₂ dissolving water (b) both rinsing with CO₂ dissolving water and drying with CO₂ gas purge.

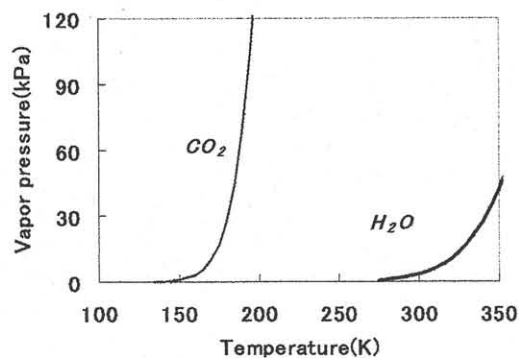


Fig.6 The vapor pressure of CO₂ and H₂O