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Impact of Gate Etch Damage and Profile in High Density DRAM Cell

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Introduction

The high density DRAM with STI(Shallow Trench Isolation) demands the long retention time due to the requirement of high speed and low power consumption. However, the presence of only a few leaky cells degrades the tail component of retention time. Especially if defect is at the drain just below gate edge under the influence of high field and high STI stress as shown in Fig.1, the deterioration of tail component in retention time becomes extremely severe. Thus, demands for low damage gate etch have increased. At the same time, high density DRAM requires high degree of etch anisotropy because poor anisotropy cause short failure between storage node plug due to BPSG(Boron Phosphorous Silicate Glass) void filled with plug poly-Si. In order to improve the degree of anisotropy, TM(Time Modulation) bias method, in which radio frequency (rf) power applied to the substrate is pulse modulated, has been suggested as shown in Fig.2 [2] Different from continuous wave(CW) bias method having only the amplitude of rf voltage as the variable parameter, TM bias method has both amplitude and the duty ratio of the pulse. The amplitude controls the energy of ions while the duty ratio controls the number of accelerated ions. In virtue of these characteristics, it has been reported that TM bias method has good anisotropy and reduce the topography dependent charging damage.[2] However, TM bias combined with high-Vpp(peak to peak value of bias voltage), especially during the overetch, causes increase of edge damage due to the increase of instantaneous acceleration ion energy. This edge damage results in deteriorating interface state at the drain just below gate edge and is closely associated with the degradation of tail component of the retention time. In this paper, device issues related to etch condition were investigated in volume production of 0.18um-DRAM. And, the bias combination mode[TM+CW bias] with high-Vpp main etch and low-Vpp overetch is proposed as the effective gate etch scheme to keep moderate profile and good retention time, for the first time.

Experimental

0.18um-rule 64Mbit DRAM with STI, in real product, was used in this experiment. Technologies are summarized in Table 2. Gate layer is composed of the 230nm-Si_3N_4/100nm-WSi/70nm-Poly Si/6.5nm-SiO_2 and the step etching method in Electron Cyclotron Resonance[ECR] plasma etching system was used. The WSi +Poly-Si film was etched with high etch rate condition(main etch) until EPD (End Point Detection). Then, the rest of layer, the partially remained Poly-Si on SiO_2 film, was etched with high selectvity condition(overetch). Two chemistry group, such as Cl_2+O_2 and HBR, were used to increase selectivity. The microwave frequency was 2.45 GHz and rf bias of 400kHz was applied to the substrate stage. Several experiments with different bias mode, including the variation of Vpp by the change of rf power was performed to verify how etch condition affects gate profile and tail component of retetion time as shown in Table1,3. Furthermore, the re-oxidation followed by gate etch was experimented to evaluate damage relief effect.

Results and Discussion

Type Ⅱ employing TM bias[30% duty ratio]+ High-Vpp for Poly-Si overetch has the superior degree of anisotropy when compared to Type Ⅰ employing conventional CW bias mode, as shown in Fig.3. The superior degree of anisotropy of Type Ⅱ is attributed to high directionality and the high energy of ions which impinge on the surface during 30% on period. The number of high energy ions are controlled by duty ratio and the deposition of $Cl_xSi_yO_z$ on sidewall and the SiO_2 surface during off period of rf bias enables to obtain high degree of anisotropy without losing selectivity. In contrast, device employing Type Ⅰ shows the severe sidecut, resulting in short failure between storage node plug due to BPSG void filled with plug poly-Si as shown in Fig.4(a),(b). In spite of this profile merit, care must be taken in applying TM bias mode to product line because the improving anisotropy by TM bias combined high-Vpp accompanies edge damage due to the increase of instantaneous acceleration ion energy. In Fig.5, device employing Type Ⅱ method shows a large etch damage when compared to device employing Type Ⅰ. In order to verify the variation of interface defect density due to edge damge, several electrical evaluation for each spliting condition was performed. Fig. 6 shows oxide leakage measured using fabricated electrode just after gate etch. Device employing TypeⅡ shows the large degradation when compared to that employing type Ⅰ. The charge pumping curve shown in Fig.7 represents that interface defect density for device employing Type Ⅰ is lower than that employing TypeⅡ. Tail component degradation of retention time for device with TypeⅡ as show in Fig.8 is attributed to interface defect increase by high Vpp-induced edge damage. Fig.9 shows that significantly deteriorated tail component of retention time could not be recovered even after re-oxidation process with different Temperature/oxidation time. Thus, we propose the modified etch method[TypeⅢ], consisting bias combination mode[TM+CW bias] with high-Vpp main etch and low-Vpp overetch . In case of TypeⅢ, high-Vpp TM bias is applied to main etch and then low-Vpp CW bias is applied to overetch. Vpp was controlled through the change of rf power as shown in Fig.11. In Fig.10, device with Type Ⅲ represents a comparable etch profile to device employing Type Ⅱ, avoiding the BPSG hole problem. In Fig.12, the localization of trapped hot carriers near the drain region was additionally evaluated. Device employing Type Ⅱ gate etch have a larger VT(threshold voltage) shift after hot carrier stressing (Vds=3.2V,Vgs=1.6V during 30sec) than that employing Type Ⅰ/Ⅲ because of the localization of trapped hot carriers near the drain region. Fig.13 shows that device with Type Ⅲ has a comparable tail component of retention time when compared to the device with Type Ⅰ. This indicates that modified etch method[Type Ⅲ] improves etch profile significantly, still keeping good retention time.

Conclusion

We propose the effective gate etching method[TypeⅢ], consisting of the bias combination mode[TM+CW bias] with high-Vpp main etch and low Vpp-overetch, for sub-micron DRAM Cell. This gate etch method[Type Ⅲ] reduces edge damage, keeping moderate anisotropy, because high Vpp-TM bias is applied to main etch and then low-Vpp CW bias is applied to overetch. This scheme contributes to avoid gate etch profile-related failure, still keeping good tail component of retention time in 64M-Bit real product.

References

[1]. S.Ueno, et al., IEEE, VLSI Tech, 2000, p84
[2]. Tetsuo Ono, et al., Sympo. On Plasma Process-Induced Damage, 1999 p167

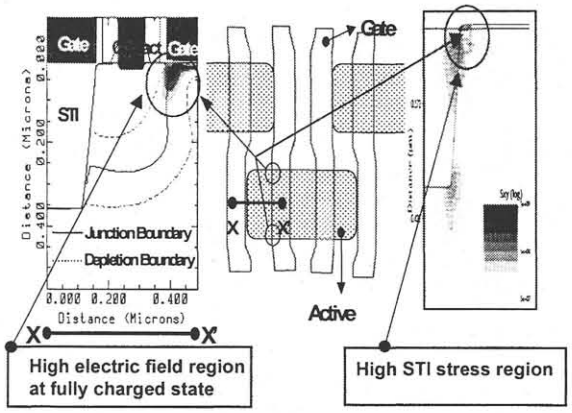


Fig.1 When defect is at the drain just below gate edge under the influence of high field and high STI stress, the deterioration of tail component in retention time become extremely severe.

Table.1 Gate etching split condition

Gate Etch	Etch Step	Mode	rf power[W]	Vpp[V]
Type I	WSi+Poly-Si [main etch]	CW	80	400
	Poly-Sioveretch	CW	35	240
	HBr-overetch	CW	20	
Type II	WSi+Poly-Si [main etch]	TM	270	1200
	Poly-Sioveretch	TM	150	930
	HBr-overetch	TM	60	630

Table.2 Technology Summary

Memory cell structure	Capacitor Over Bit Line
Design rule	0.18um
Isolation	Shallow Trench Isolation
Gate oxide thickness	6.5nm
Gate stack layer	Wsi/poly/SiO2
Cell Storage Node Contact	SAC (Self-Aligned Contact)
Capacitor dielectric	ON dielectric

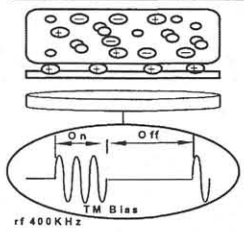
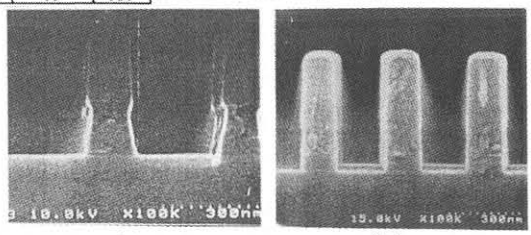
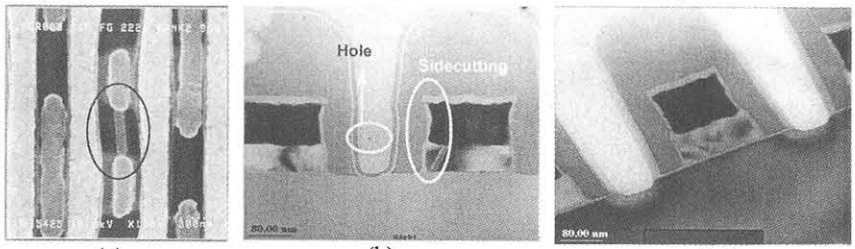


Fig.2 Schematic concept of TM bias in ECR plasma etching system.



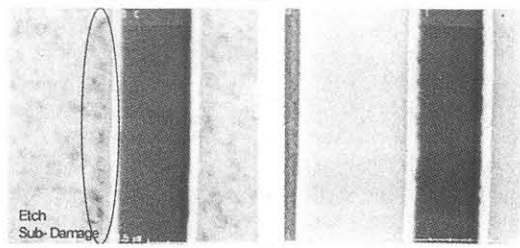
(a) (b)

Fig.3 SEM image of gate profile due to gate etch method. The improvement in degree of anisotropy was obtained by TM bias . (a) Type I (b) Type II



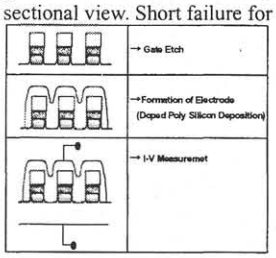
(a) (b) (c)

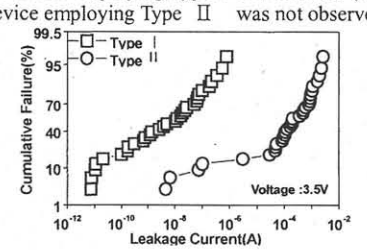
Fig.4 Short failure between storage node plug due to BPSG void filled with plug Poly-Si due to gate etch method was obserbed for device employing Type I etch method. (a) Top-view (b) Cross sectional view. Short failure for device employing Type II was not observed in (c)



(a) (b)

Fig.5 The comparison of edge damage due to to gate etch method. Device employing Type II (a) shows a large etch damage when compared to device employing Type I (b).





(a) (b)

Fig.6 To verify gate edge damage, oxide leakage was measured using fabricated electrode just after gate etch. Device with Type II shows the larger degradation when compared to that with type I .
(a) Pattern Fabrication (b) Oxide leakage

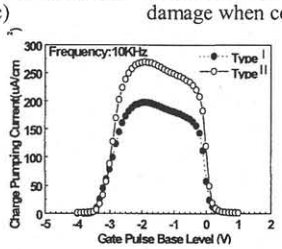


Fig.7 Charge pumping current measured for cell transistors with gate etch Type I and Type II, respectively.

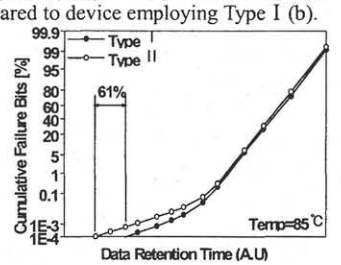


Fig.8 Device with Type II showed a considerable decrease of the tail component of retention time compared to that with Type I

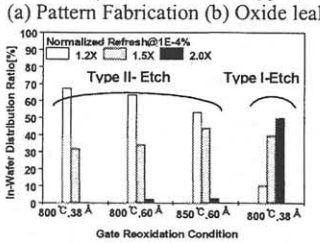


Fig.9 Significantly deteriorated tail component could not be recovered even after re-oxidation process.

Table.3 Proposed gate ething Method

Gate Etch	Etch Step	Mode	rf power[W]	Vpp[V]
Type III	WSi+Poly-Si [main etch]	TM	270	1200
	Poly-Sioveretch	CW	35	240
	HBr-overetch	CW	30	270

Proposed Type III method consists of the bias combination mode[TM+CW bias] with high-Vpp mainetch and low Vpp-overetch

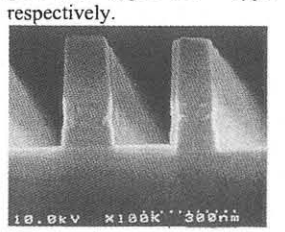


Fig.10 Device with Type III represents a comparable etch profile to device with Type II

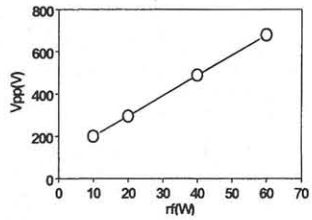
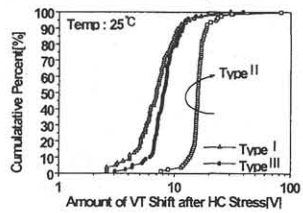
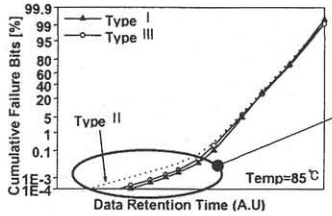
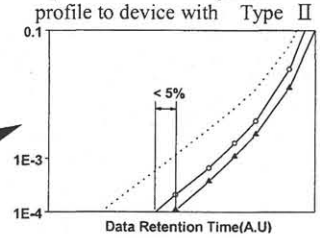


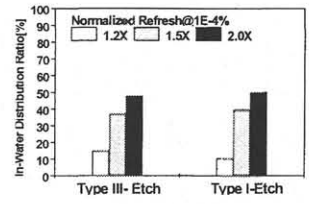
Fig.11 Vpp is controlled through the change of rf power







(a)



(b)

Fig.12 VT shift due to the localization of trapped hot carriers near the drain region.

Fig.13 Device with Type III has a comparable tail component of retention time when compared to the device with Type I . (a) Cumulative retention time (b) Distribution ratio of tail component of retention time in wafer.