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Effect of Poly Metal Gate Etch Post-Cleaning on the Tail Distribution of DRAM Data Retention Time

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Introduction

As the memory density in DRAM increases, the resistance of a word line significantly increases and the gate RC delay is placing serious limitations on device performance. The use of metal gate is one of the solutions to this problem. Tungsten has been widely studied as the gate material among many other choices, due to its low resistivity and thermal stability[1-2]. However, the process incompatibility with respect to the conventional polycide gate process has been giving rise to the issue of data retention time in DRAM cells among many other device characteristics. For example, the conventional polycide gate etch post-cleaning condition (the chemical containing H_2O_2) followed by the metal gate patterning could not be used because it corrodes the metal layer. The cleaning process after gate etching is a necessity for effectively removing unwanted byproducts generated by gate etch process. Therefore, optimizing the cleaning condition in the poly metal gate is an important subject, associated with data retention time as well as cell transistor characteristics such as threshold voltage shift and hot carrier degradation. In this paper, we have investigated, for the first time, the effect of post-cleaning process after gate patterning on the tail distribution of data retention time in DRAM cells having poly metal (W/WN/poly-Si) gate. And also, we propose the optimized gate etch post-cleaning condition in poly metal gate device to guarantee the characteristics of DRAM data retention time comparable to that of the conventional polycide gate etch post-cleaning process.

Experimental

The devices were manufactured using a 0.18um technology which is quite stable in terms of technology maturity. In order to verify how poly metal gate etch post-cleaning process affects the tail component of data retention time distribution, two groups of samples were prepared. Group-1 was fabricated using a conventional polycide gate with a already confirmed etch post-cleaning process through several generations and several different conditions for poly metal gate etch post-cleaning, and group-2 was manufactured using W/WN/poly-Si stacked poly metal gate with several different etch post-cleaning processes to investigate the effect of gate etch post-cleaning condition on data retention time, practically. The detailed process and electrical bias conditions used in this experiment were summarized in Table 1.

Results and Discussion

Fig.1 shows the TEM cross sectional images for gate etch post-cleaning conditions(type-A and type-B) in actual poly metal gate devices, respectively. Type-A provides thicker oxide layer on the sidewall and at the bottom of spacer because of the remaining residue due to the poor capability of etch byproducts removal, in addition to the thermally grown oxide layer by selective reoxidation. On the contrary, type-B shows thinner oxide layer even though selective reoxidation was done because of good removal ability of etch byproducts. Previous research[3] on the characterization of the unwanted etch byproduct using Auger Electron Spectroscopy(AES) reveals that it is mainly composed of the low density SiOx with a few trace elements, generated upon the reaction between oxygen in the etchant gas and the poly-Si. The role of the generated interface states on the gate-induced drain leakage (GIDL) current has been previously studied[4] and the interface trap is thought to induce thermionic field emission (TFE) current in off-state MOSFET's[5]. It has been also reported that GIDL current has a dominant impact on tail component of data retention time in DRAM cells[6]. On the basis of these studies, we assumed the schematic drawing of the relation between etch byproducts and tail component of retention time as shown in Fig.2. That is, the byproducts generated by gate etch process induce the increase of interface contamination and trap sites, resulting the increase in the anomalous leakage current and deteriorating the tail component of data retention time. In order to evaluate the effect of etch residue remained at the gate edge on data retention time as well as cell transistor characteristics, first, we investigated the characteristics of cell transistor and data retention time for etch post-cleaning conditions in group-1 device having a conventional polycide gate. The cumulative characteristics of cell transistor hot carrier degradation for gate etch post-cleaning conditions was shown in Fig.3. The degradation of threshold voltage before and after hot carrier stress (under the bias condition set at the peak substrate current,Vds=3.2V and Vgs=1.6V for 30sec) in type-A condition was extremely severe. While type-B condition shows the similar hot carrier characteristics to that of reference condition. It is observed that the initial degradation from hot carrier stress in type-B is much lower, implying that the device has fewer initial interface trap and lower interface contamination at the gate edge. Charge pumping method showing the interface state density at the gate edge and under the sidewall region confirms the fact that an initial interface state of type-B is lower as shown in Fig.4. To verify the relation between the GIDL current and tail component of data retention time, we examined the cumulative characteristics of GIDL current measured at Vds=5V from the difference between gate floating and gate zero bias condition using 64Kbits cell-array pattern as shown in Fig.5. It was found that the GIDL current of type-B without etch residue decreased due to the decrease of interface trap sites and interface contamination. And in-wafer mapping, uniformity and frequency distribution results as well as cumulative probability characteristics of retention time failure bits(@1E-4%) for gate etch post-cleaning conditions were characterized as presented in Fig.6. The results of Fig.5 and Fig.6 show that type-B is much better condition. And also, the good agreement of GIDL current and tail component of retention time characteristics was obtained. In terms of the post-cleaning process after gate patterning, the present experimental results confirm the hypothesis that the removal of the damaged oxide improves the interface quality of the remaining oxide, resulting in reducing GIDL current and then improving the tail component of data retention time. Consequently, we could find that type-B as poly metal gate etch post-cleaning condition is comparable to reference condition. And practically, we have verified that type-B condition has the reduced GIDL current and the improved tail component (50%) of data retention time distribution in an actual poly metal gate device(group-2) as illustrated in Fig.7 and Fig.8.

Conclusion

We have investigated the impact of gate etch post-cleaning process on the tail distribution of data retention time in DRAM cells having poly metal gate for the first time. By optimizing the cleaning process after poly metal gate patterning, the poly metal gate device with greatly improved tail component of retention time characteristics was obtained. In particular, we propose the optimized poly metal gate etch post-cleaning condition to guarantee the characteristics of DRAM data retention time comparable to that of the conventional polycide gate etch post-cleaning process.

References

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[2]. B.H. Lee, *et al.*, IEEE, IEDM Tech. Dig. 1998, p385
[3]. J.H Kim, *et al.*, IEEE, ICVC Tech. Dig. 1999, p487
[4]. G.Q. Lo, *et al.*, IEEE, IEDM Tech. Dig.1990, p557
[5]. T.W., *et al.*, IEEE, IEDM Tech. Dig. 1994, p161
[6]. K. Saino, *et al.*, IEEE, IEDM Tech. Dig. 2000

Item	Group-1			Group-2	
Design Rule	0.18um				
Isolation	Shallow Trench Isolation(STI)				
Gate Material	W-polycide			W/WN/poly-Si	
Gate etch post-cleaning condition (Oxide removal rate)	Reference (1 Å/min)	Type-A (0 Å/min)	Type-B (1 Å/min)	Type-A (0 Å/min)	Type-B (1 Å/min)

Supply Voltage	Vdd = 1.8V
Substrate Volatge	Vsub = -1.0V
Word Line Boost Voltage	Vboost = 3.6V
Plate Voltage	Vpl = 0.9V

Table 1. Detailed process splitting and electrical bias conditions used in the experiment . The oxide removal rate of type-B condition is comparable to reference condition.

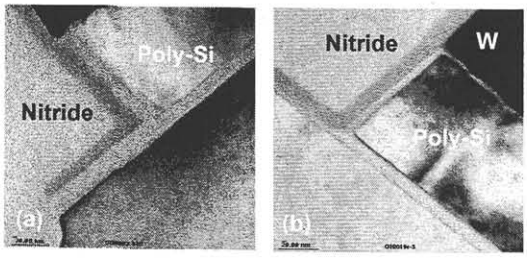


Fig.1 TEM images of devices having different poly metal (W/WN/poly-Si) gate etch post-cleaning conditions after full process intergration. Both type-A(a) and type-B(b) were applied selective reoxidation.. Type-B(b) shows thinner oxider layer because of good removal ability of byproducts.

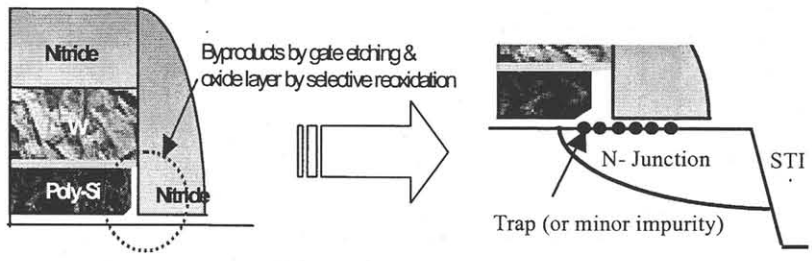


Fig2. Schematic illustration of the relation between etch byproducts(generated after gate patterning) and tail component of retention time(tREF) in DRAM cells.

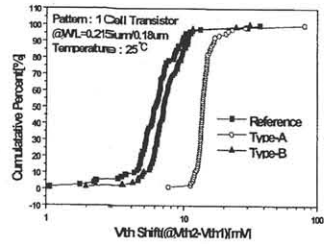
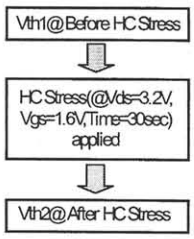


Fig.3 Cumulative characteristics of cell transistor hot carrier degradation for each splitting process having different gate etch post-cleaning conditions in ploycide gate device.



(Evaluation method and sequence of cell transistor hot carrier degradation)

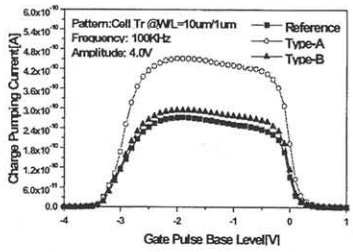


Fig.4 Charge pumping current as a function of gate pulse base voltage. The measured device has polycide gate with width of 10um and length of 1um.

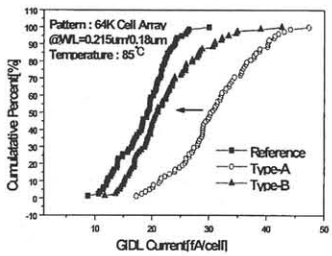
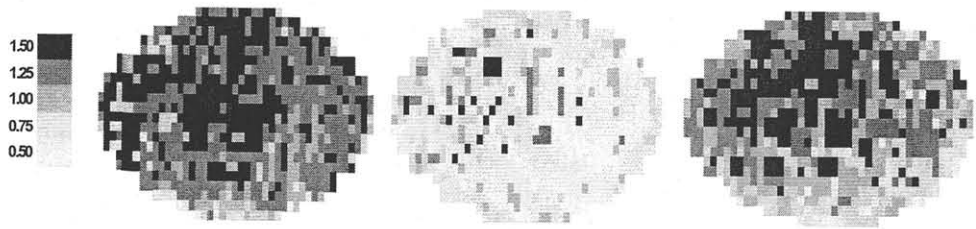


Fig.5 Cumulative characteristics of GIDL current(at Vds=5V) in cell transistor for etch post-cleaning conditions in devices having conventional polycide gate.



(a) Reference (b) Type-A (c) Type-B

Fig.6 Characteristics of data retention time for gate etch post-cleanings in conventional polycide gate(group-1). In-wafer mapping & uniformity results of tREF failure bits(@1E-4%) for each gate post-cleaning condition(a), (b) and (c). The frequency of tREF(@1E-4%) in wafer for gate each post-cleaning condition was shown in figure (d). The cumulative probability of tREF for each condition was illustrated in figure (e).

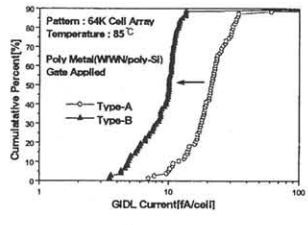
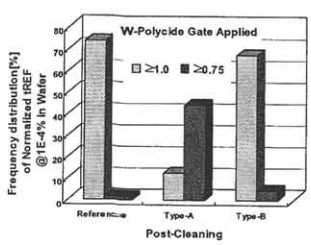
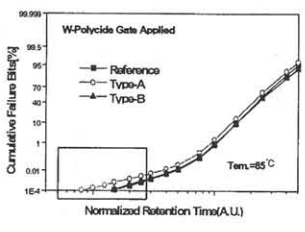


Fig.7 Cumulative characteristics of GIDL in cell transistor for etch post-cleanings in poly metal gate device.



(d) Frequency distribution of tREF in wafer for each post-cleaning.



(e) Characteristics of cumulative tREF for each post-cleaning.

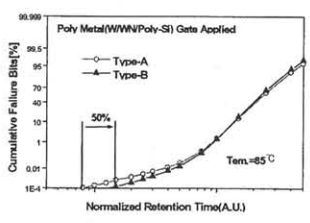


Fig.8 Characteristics of cumulative tREF for gate etch post-cleanings in poly metal gate device.