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Filling of Tungsten into Deep Trench Using Time-Modulation CVD Method

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1. Introduction

Three-dimensional (3D) integrated microsystems such as 3D LSI, 3D package and 3D MEMS have attracted much attention as one of the candidates to achieve new integrated microsystem in a post-SoC era. However, several new technologies have to be developed in order to realize such 3D integrated microsystems. The most important one of these new technologies is the vertical interconnection. A huge number of vertical interconnections are formed in 3D integrated microsystems. Therefore, the performance of 3D integrated microsystem is significantly influenced by the data transfer speed of vertical interconnection. In order to increase the data transfer speed of vertical interconnection, the resistance and capacitance of vertical interconnection should be minimized. Then, in this paper, the process technology to minimize the resistance of vertical interconnection is discussed focusing on 3D LSI.

2. Experiments

We have succeeded in fabricating a 3D LSI as shown in Fig.1 using a new wafer stacking technology [1), 2)]. An LSI wafer with buried vertical interconnections is thinned from the backside and then stacked another LSI wafer in our wafer stacking technology. The electrical connection between the upper and lower wafers is achieved by low resistive poly-Si buried vertical interconnections. We can completely fill poly-Si into deep trench with very high aspect ratio as shown in Fig.2 where the diameter and the depth of trench are 2 μ m and 50 μ m, respectively. The heavily phosphorus doped poly-Si was deposited into the trench using low pressure CVD method after forming the thermal oxide with the thickness of 0.6 μ m on the trench surface. As a result, the vertical interconnection resistance of 30 Ω was obtained. This resistance value is too high to achieve a high speed 3D LSI. Then, we try to employ tungsten in place of poly-Si for buried vertical interconnection. Tungsten film was deposited into the trench using a time-modulation low pressure CVD method. The multi chamber reactor is used in our W-CVD equipment as shown in Fig.3. The reaction chamber is a cold wall type and was maintained at high vacuum state of around 5×10^{-6} Pa. The wafer temperature was maintained at 350℃. Figure 4 shows the gas flow sequence in our time-modulation CVD for tungsten. The reaction mechanism corresponding to this gas flow sequence is illustrated in Fig.5. WF_6 (10 sccm) and SiH_4 (5 sccm) gases are alternately introduced into the reaction chamber in our time-modulation W-CVD method. One gas flow cycle consists of the introduction of WF_6 and the evacuation of WF_6 followed by the introduction of SiH_4 and the evacuation of SiH_4. In Fig.4, the duration time t_E after turning off WF_6 flow is necessary to evacuate remaining WF_6 gas so that undesirable reaction between WF_6 gas and SiH_4 gas inside the chamber is prohibited. The duration time t_E after turning off SiH_4 flow is needed to promptly evacuate the reaction byproducts inside the deep trench. Accordingly, in our time-modulation W-CVD method, after the adsorption of WF_6 gas on the trench surface by introducing WF_6 gas into the chamber, extra WF_6 gas remaining in the chamber is evacuated and then SiH_4 gas is introduced to reduce WF_6 by SiH_4 as shown in Fig.5. The reaction byproducts such as SiF_4, HF and H_2 are produced inside the deep trench as a result of the reduction of WF_6 by SiH_4 [3)]. These reaction byproducts inside the deep trench are promptly evacuated by stopping the supply of SiH_4 gas as shown in Fig.5.

3. Results and Discussion

A deep Si trench with the diameter of 2 μ m and the depth of 50 μ m was formed by inductivity coupled plasma (ICP) etching and then 0.5 μ m thick poly-Si was deposited after the formation of 0.6 μ m thermal oxide. As a result, the diameter of trench decreases to 1 μ m. Tungsten was deposited into such thinned trench. Fig.6 shows an SEM cross-section of tungsten (W) buried vertical interconnection formed using a conventional low pressure W-CVD method where both gases of WF_6 and SiH_4 are simultaneously and continuously introduced into the reaction chamber. A very poor W filling characteristic was obtained as is obvious in the figure. Such poor filling characteristic is caused by the reaction byproducts remaining inside the trench which prevent WF_6 gas from penetrating deeply toward the bottom of trench. On the other hand, an excellent W filling characteristic was obtained as shown in Fig.7 when the time-modulation W-CVD method was used. A very thin and deep trench with the diameter of 1 μ m and the depth of 50 μ m was completely filled with tungsten as is obvious in the figure. The resistivity of deposited W film was 20 $\mu\Omega$-cm. Thus, we could fabricate a W buried vertical interconnection with the resistance more than one order of magnitude lower than that of poly-Si vertical interconnection as shown in Fig.8.

4. Conclusion

We have succeeded in completely filling tungsten into a deep trench with the diameter of 1 μ m and the depth of 50 μ m using the time-modulation W-CVD method. As a result, we could fabricate a W buried vertical interconnection with a very low resistance for 3D LSIs.

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References:

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2) K. W. Lee *et al.*, IEDM'00. p165(2000).

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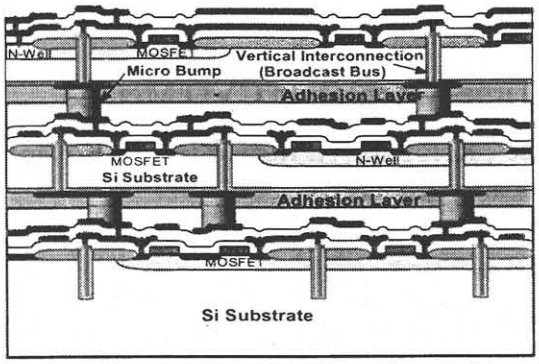

Fig 1. Cross-sectional structure of 3D LSI.

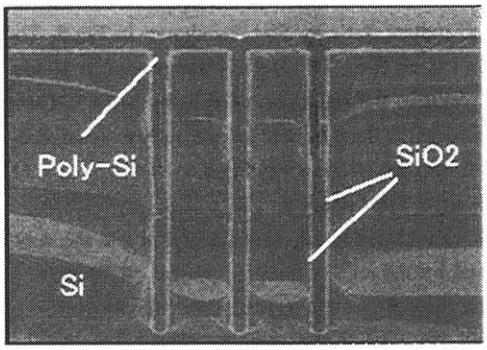

Fig 2. SEM cross-sectional view of poly-Si buried vertical interconnection.

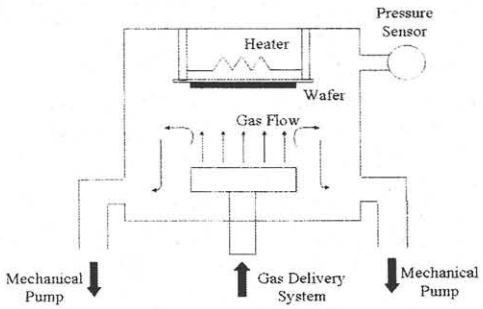

Fig 3. Schematic structure of W-CVD equipment.

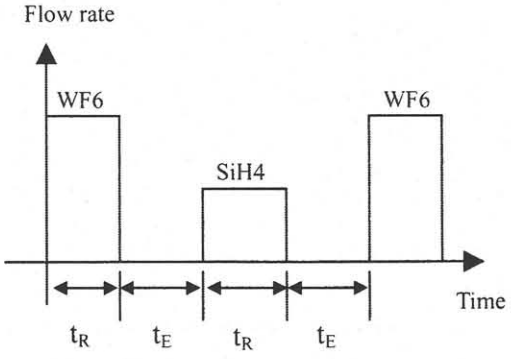

Fig 4. Gas flow sequence in time-modulation W-CVD.

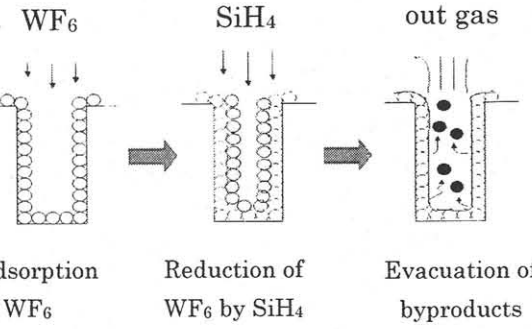

Fig 5. Reaction mechanism for time-modulation W-CVD.

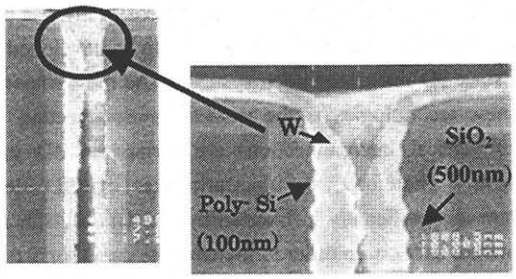

Fig 6. SEM cross-sectional view of W buried vertical interconnection with void.

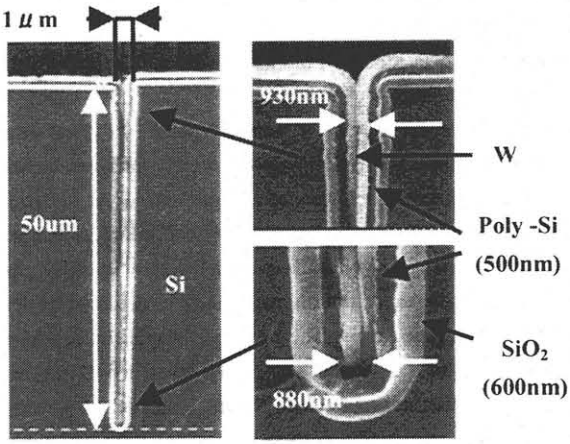

Fig 7. SEM cross-sectional view of W buried vertical interconnection without void.

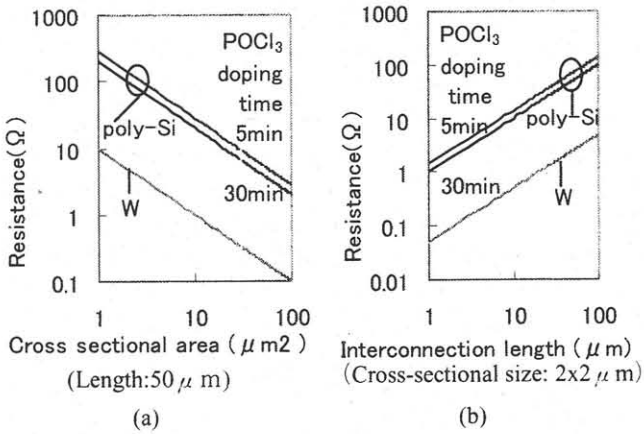

Fig 8. Resistance of poly-Si and tungsten vertical interconnections.