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Ultrathin Nitride/Oxide Stack Gate Dielectric (14.9Å to 20.3Å) for Sub-0.13 μm CMOS and Beyond

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1. Introduction

The aggressive scaling on gate oxide thickness has imposed a severe challenge to Moore's Law due to excessive direct tunneling current. The development of high-K gate dielectric is still far from device realization [1]. Silicon nitride has been suggested as an immediate solution due to lower tunneling current, strong resistance to boron penetration and simple process integration [2-3].

The implementation of silicon nitride gate dielectric requires an ultrathin interfacial oxide layer due to its poor interface with silicon substrate. A novel method has been proposed to realize the interfacial oxide by N_2O post oxidation of NH_3-nitrided Si [4]. In this paper, we propose an improved process by *in-situ* steam oxidation of CVD nitride with better oxide integrity and excellent device performance.

2. Experimental

Both n-channel and p-channel devices were fabricated by a standard 0.13μm CMOS process. Silicon nitride was deposited by a CVD system at 750 °C, 10-40 torr for 15-30 seconds using NH_3 and SiH_4. Subsequent to Si_3N_4 deposition, interfacial oxide was formed by either N_2O oxidation [4] at 950°C or *in-situ* steam oxidation (950°C, H_2/O_2=2:98) with various process durations. This was followed by N_2 annealing at 1000 °C for 20 seconds. Equivalent oxide thickness (EOT) was extracted at strong accumulation by considering quantum mechanical effect [5].

3. Results and Discussion

Figures 1 and 2 show the high frequency C-V curves of N/O stack with N_2O oxidation (EOT=20.2Å) and N/O stack with $H_2(2\%)/O_2$ oxidation (EOT=14.9Å), respectively. Negligible hysteresis is observed for both devices, indicating effective bulk traps elimination in the CVD nitride by both processes. The gate leakage current at accumulation for both nMOS and pMOS is depicted in Figs. 3 and 4 respectively. It is shown that the gate leakage is significantly reduced as compared to SiO_2. The tunneling current is found to be ~1mA/cm^2 at Vg=-1V for EOT=14.9 Å, comparable to the published data on RTCVD nitride and JVD nitride in [3]. Additionally, the N/O gate stack with *in-situ* steam oxidation shows a lower leakage current (~2x) as compared to its N_2O counterpart although they have identical EOT.

Stress induced leakage current (SILC) for both N/O gate stack processes is shown in Fig. 5, indicating that the *in-situ* steam oxidation has a smaller ΔJ_g and hence lower defect generation rate. Figures 6 and 7 show time to breakdown (T_{BD}) distribution under constant voltage stressing by using soft breakdown as breakdown criteria. It is shown that N/O gate stack by *in-situ* steam oxidation has significantly higher T_{BD} than the N_2O oxidation for both NCAP and PCAP, possibly due to lower injected current density (Figs. 3 & 4) and lower defect generation rate (Fig. 5). This reliability improvement can be further explained by more effective structural defect elimination by atomic oxygen generated in the $H_2(2\%)/O_2$ ambient [6].

Figure 8 shows that the normalized transconductance (GmxTox) for N/O gate stack by *in-situ* steam oxidation and N_2O oxidation are comparable, implying similar mobility. Figures 9 and 10 show the typical Ids-Vds and Ids-Vgs characteristics for N/O gate stack with EOT=14.9 Å for 0.12μm MOSFET. Excellent drive current is achieved. Good subthreshold characteristics are observed for both nMOSFET and pMOSFET with swing as 79.8 mV/dec and 75.9 mV/dec respectively. Hot carrier reliability (HCI) for nMOSFET and negative bias temperature instability (NBTI) for pMOSFET have been performed for both N/O gate stack process, as illustrated in Figs. 11 and 12. The *in-situ* steam oxidation shows less degradation in Ids and Gm than the N_2O, suggesting a better interface hardness formed by $H_2(2\%)/O_2$ oxidation.

4. Conclusion

We have reported a new and improved N/O stack gate dielectric process by first depositing a CVD nitride followed by *in-situ* steam oxidation. Negligible bulk traps, low gate leakage current (~1mA/cm^2 @V_g= -1V for EOT=14.9Å nMOSFET), superior gate oxide integrity, and improved HCI and NBTI reliability have been achieved. High drive current and good subthreshold characteristics have been demonstrated for sub-0.13μm MOSFETs.

References

[1] International Technology Roadmaps for Semiconductors 2000 update.
[2] X. Qiang, *et al., IEDM Tech. Dig.*, p.860, 2000.
[3] Q. Lu, *et al., International Semiconductor Device Research Conference*, p.489, 1999.
[4] S. C. Song, *et al., Symp. on VLSI Tech*, p.137, 1999.
[5] K. Yang, *et al., Symp. on VLSI Tech.*, p.77. 1999.
[6] T. Y. Luo *et al., IEEE Electron Device Lett.*, vol.21, p.382, 2000.

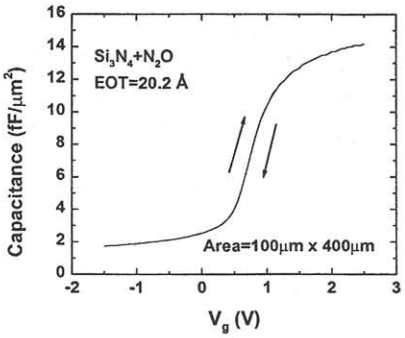

Fig.1 Hysteresis characteristic of N/O stack gate dielectric by Si_3N_4+N_2O (EOT=20.4Å). No measurable hysteresis indicates negligible bulk trap in the stack.

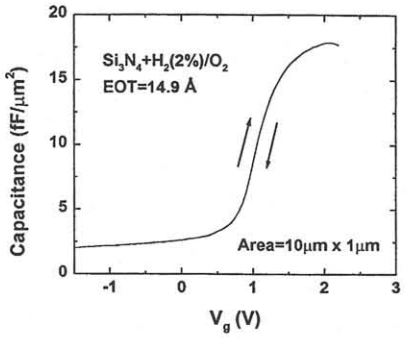

Fig.2 Negligible hysteresis for N/O stack gate dielectric by Si_3N_4+H_2(2%)/O_2 (EOT=14.9Å). Roll off at strong accumulation is due to high leakage current.

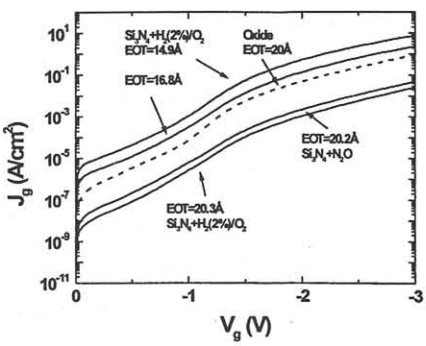

Fig.3 J-V curves of N/O stack with EOT ranging from 14.9 Å to 20.3 Å for nMOS. J_g=1mA/cm^2 @V_g=-1V for EOT=14.9 Å.

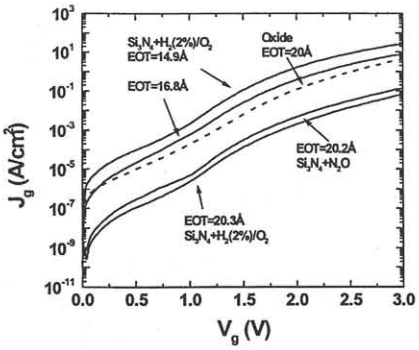

Fig.4 J-V curves of N/O stack with EOT ranging from 14.9 Å to 20.3 Å for pMOS. J_g=2mA/cm^2 @V_g=1V for EOT=14.9 Å.

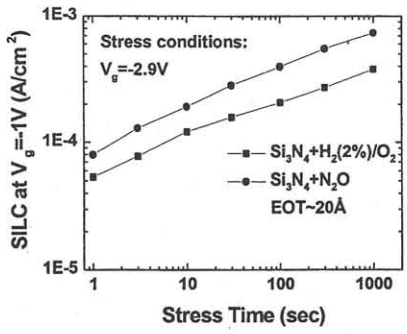

Fig.5 *In-situ* steam oxidized device shows a lower SILC for nMOS 400μm x 100μm, indicating a lower defect generation rate.

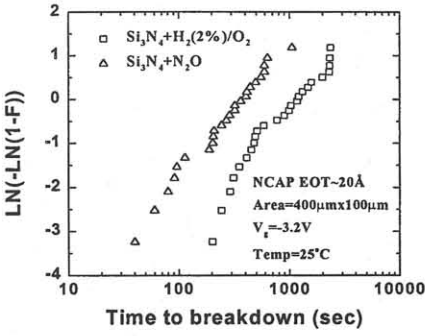

Fig.6 Time to breakdown for nMOS capacitors shows better reliability for *in-situ* steam annealing.

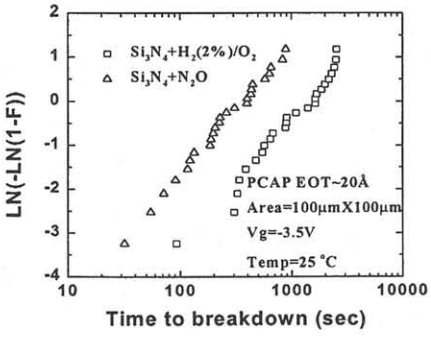

Fig.7 Improved time to breakdown is also achieved for pMOS capacitors with *in-situ* steam oxidation.

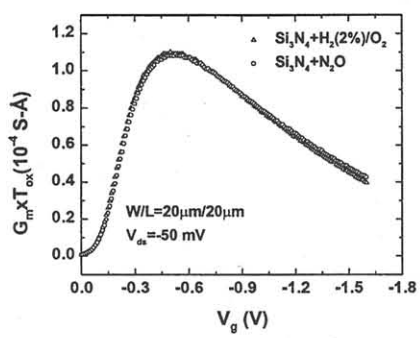

Fig.8 Both process conditions show essentially the same channel mobility.

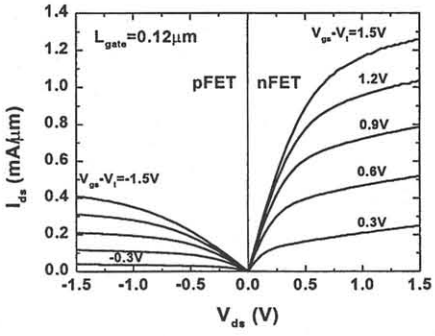

Fig.9 Ids-Vds characteristics of 0.12μm MOSFET with N/O gate stack (EOT=14.9 Å).

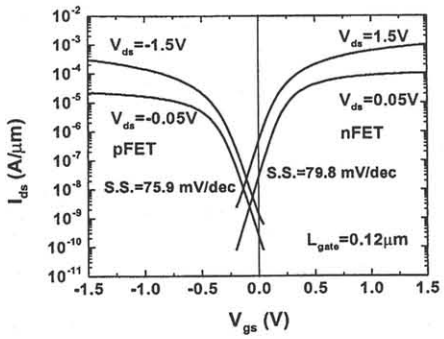

Fig.10 Subthreshold characteristics of 0.12μm MOSFET with N/O gate stack (EOT=14.9 Å).

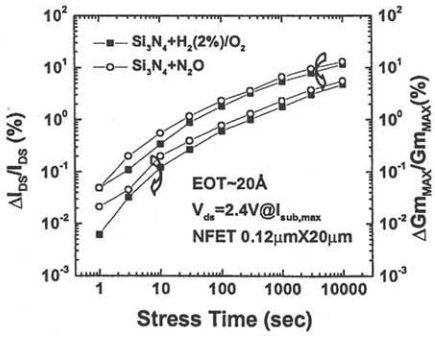

Fig.11 *In-situ* steam oxidation shows less degradation in Ids and Gm,max for 0.12μm x20μm nMOSFET under Vds=2.4V@Isub,max.

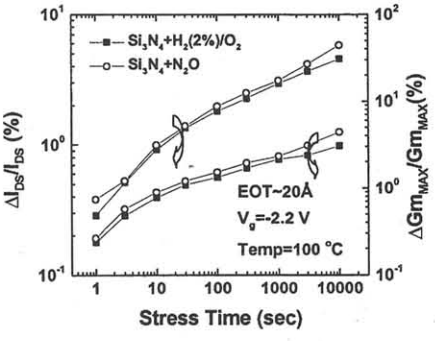

Fig.12 Ids and Gm degradation induced by NBTI under Vg=-2.2V and 100 °C for 0.12μm x 20 μm pMOSFET.