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Highly Reliable MOS Trench Gate FET by Oxygen Radical Oxidation

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1. Introduction

Trench gate MOS FET[1] and vertical channel MOS FET[2] are effective device structures to minimize the short channel effect [1] or to keep its sufficient channel length regardless of scaling lateral dimensions[2]. Since thermally grown gate oxides have non-uniform thickness and poor integrities on (110) or (111) surface along with 3-D patterned substrate, these 3D devices have resulted in having complicated process steps to manage these issues. The oxygen radical oxidation process at around 400°C by microwave-excited high-density Kr/O_2 plasma without metallic contaminations and substrate surface damages due to its very low electron temperatures of around 0.7eV, realizes high quality gate oxide on the (111) surface with the (100) surface equivalent oxide integrity [3,4]. In this paper, for the first time, we propose the advantages of the oxygen radical oxidation process for the highly scalable and reliable high voltage trench gate MOS FET for system LSI and flash memory, with excellent oxide coverage, and hot electron stress immunity.

2. Experiment

Oxygen radical gate oxides were grown by microwave -excited high-density plasma system at 400°C in Kr/O_2 mixed gases ambient, where huge amount of oxygen radicals are generated by collisions between intermediate excited Kr* and oxygen molecules. Capacitors with shallow trench gate oxides formed by the oxygen radical oxidation and conventional thermal oxidation, and trench MOS FETs by the conventional thermal oxidation has been fabricated by the process flow in Fig.1. Planar type NMOS FETs on (100) and (111) surface orientation has fabricated for hot electron evaluation.

3. Results and Discussion

It has shown in Fig.2 that the oxide thickness of Kr/O_2 plasma oxidation do not depend on the silicon surface orientation of (100), (111), and (110) up to about 15nm, while the dry O_2 oxidation at 900°C shows 50% thicker oxide on non-(100) surface. Fig.3 and 4 show TEM images of trench corner region by Kr/O_2 plasma oxidation, respectively. These results exhibit very smooth and uniform coverage of SiO_2 films in spite of gradually changing silicon surface orientation from (100) on the bottom to (110) on the sidewall via (111) at the corner. While, the dry O_2 oxidation at 900°C results in 50% thicker oxides on the sidewall than on the bottom and local thinning spot in the corner region (Fig.5). This leads degradations of break-down voltage, TDDB of the trench gate oxide, and the performance of the trench MOS FETs. As shown in Fig. 6, with the conventional thermal gate oxide, the sub-threshold slope of the trench MOS FET is 140mV/decade, which is worse than 100mV/decade of the planer type. Simulated results in Fig.7(a), (b) show that the thickness uniformity of the trench side wall and bottom can improve the performance of trench MOS FET, such as drain current, sub-threshold slope, and Vth. The hot electron stress life time of MOS FETs fabricated on (111) surface shows large improvement by the Kr/O_2 plasma gate oxidation and close to that on (100) surface by the thermal gate oxide (Fig.8). The trench MOS FET exhibits very strong short channel effect suppression in roll off characteristics of Vth and S/D punch through voltage without any scaling of gate oxide thickness and operation voltage (Fig. 9).

4. Conclusions

Silicon oxide grown by Kr/O_2 high-density plasma at 400°C has been confirmed to provide excellent coverage and uniformity on any surface orientations inside the trench, and hot electron immunity on (111) surface. This realizes high performance and reliable 3D devices, such as the trench gate MOS FET, which can shrink gate length to 0.1μm with high voltage operation by low cost process integration. This technology is quite applicable to high voltage circuits in the system LSI and flash memory.

References

[1] S. Nishimatsu et al., Jpn, J. Appl. Phys., 16; 179, (1977)
[2] H.Takato et al., IEDM, p222 (1988)
[3] M.Hirayama et al., IEDM, p249 (1999)
[4] Y.Saito et al., Symposium on VLSI Technology p176 (2000)

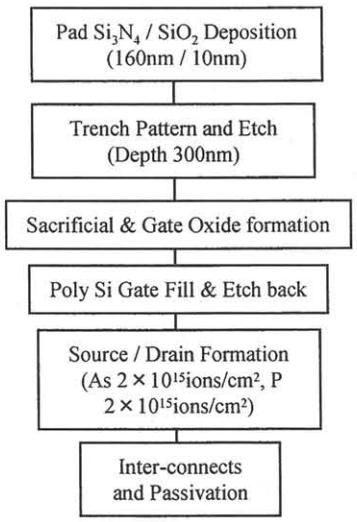


Fig.1 Outline process flow of experiment

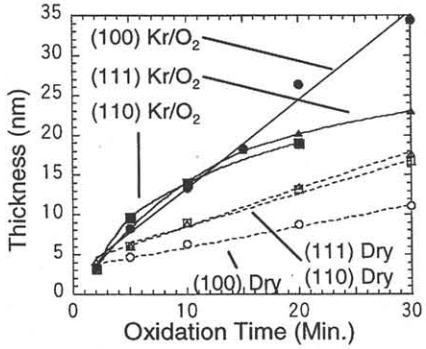


Fig.2 Dependence of oxidation rate of Kr/O_2 plasma 400℃ and dry O_2 900℃ on Si surface orientation.

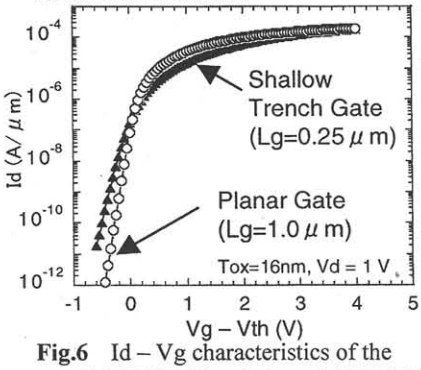


Fig.6 Id – Vg characteristics of the trench MOS FET and planar MOS FET with thermally formed gate oxide.

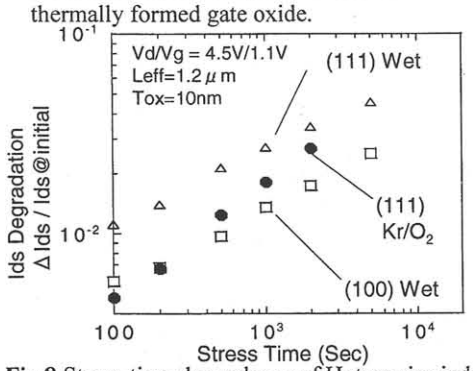


Fig.8 Stress-time dependence of Hot-carrier-induced Ids degradation for NMOS FETs fabricated by (100) Wet 700℃, (111) Wet 700℃, and (111) $Kr/O_2$400℃ oxidation.

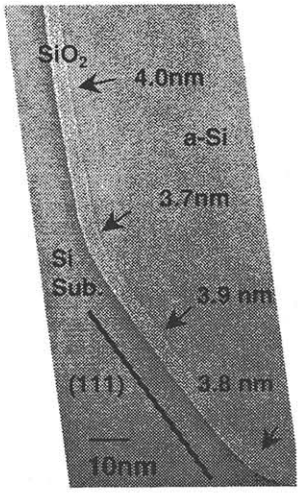
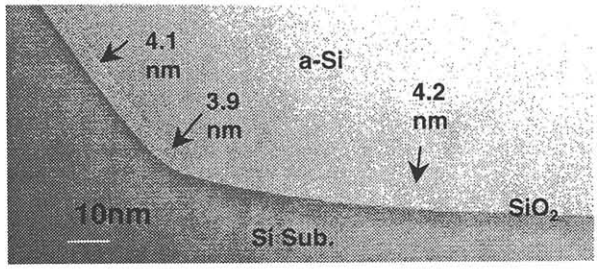


Fig.3 Cross sectional TEM view of 4.2nm thick oxide grown by Kr/O_2 plasma 400 ℃
←(a) Trench side wall & corner region
↓ (b) Trench bottom & corner region



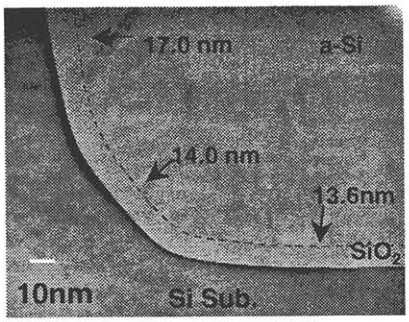


Fig.4 Cross sectional TEM view of 14nm thick oxide grown by Kr/O_2 plasma 400 ℃ inside trench.

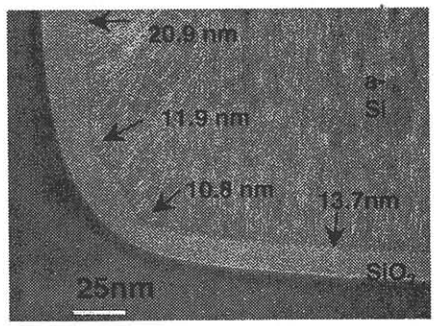
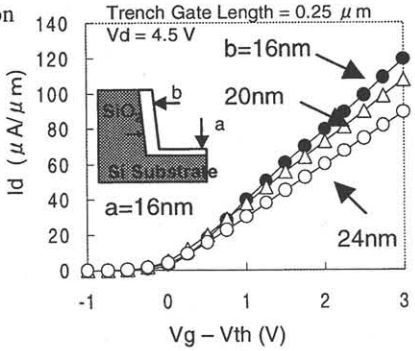


Fig.5 Cross sectional TEM view of 14nm thick oxide grown by dry O_2 900 ℃ inside trench.



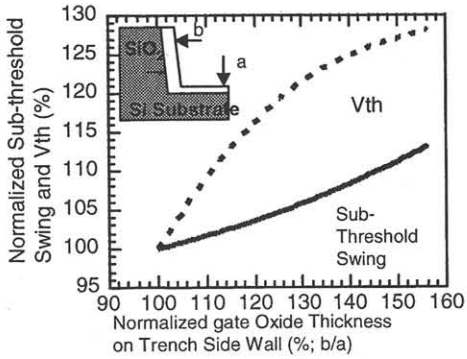
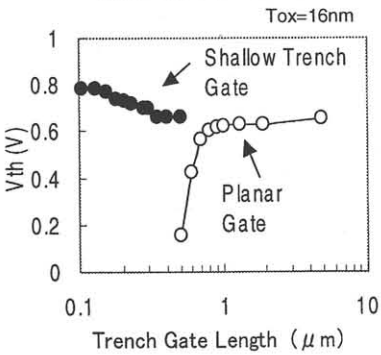


Fig.7 Simulated Id and sub-threshold swing improvement by gate oxide thickness control at side wall of trench. Bottom oxide thickness is 16nm .



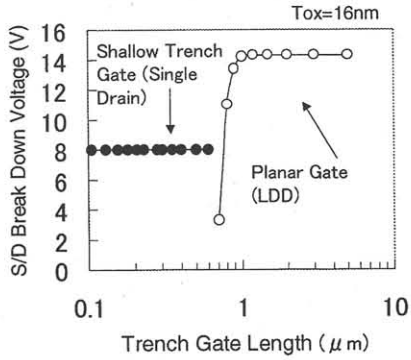


Fig.9 Vth and S/D breakdown voltage roll-off by gate length of trench gate and planar NMOS FET, both by thermal gate oxidation. S/D break down voltage at the trench gate is limited by drain to sub break down.