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Repeated Spike Technology Employed in Rapid Thermal Processing

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1. Introduction

Rapid thermal processing (RTP) has been used widely in Ultra large scaled integrated circuit technology (ULSI) because of its small thermal budget. A technology called repeated spike which is characterized by setting the temperature to ramp up and down during process, like a trapezoid wave, has been employed for RTP system. It had been investigated that repeated spike oxidation (RSO) can improve gate oxide thickness uniformity.[1]In this work, the oxide reliability prepared by RSO was studied with the comparison of conventional oxidation method. In addition, repeated spike treatment (RST) was carried out in nitrogen before oxidation. The oxide and silicon wafer after RST also exhibits obvious different behavior with respect to conventional ones.

2. Experimental

Figure1(a) and (b) show the representive temperature profiles for repeated spike and typical cases, respectively. It should be noticed that RSO has a relative low average process temperature than the typical case. The oxygen pressure was set to be 80 torr. The typical samples were oxidized using the profile in fig1(b) by kept the temperature at 700℃ for 20, 40, and 60 sec. RSO was performed using the profile in Fig.1(a) by repeat the spike for 3, 5, and 7 times.

The RST+O samples were treated by the profile in Fig.1(a) and then oxidized in 30 torr oxygen at 850℃ for 10, 20, and 30 sec.. The Typical+O samples were prepared like the RST+O but the treatment profile before oxidation is Fig.1(b).

3. Results and Discussions

Figure2 shows the comparison in tunneling current of RSO and Typical Samples. It is observed that around the similar oxide thickness, the tunneling current of RSO samples are 2 to 3 orders lower than Typical samples. The I-V curves of typical and RSO samples under the 1st and the 10th measurement on the same tested device is shown in the inset of Fig.1. Since there is little difference between the 1st and the 10th measurement, the reduction in tunneling current of RSO sample is not due to the electron trapping during measurement. From Fig.3, the Weibull plot of tunneling current for RSO and Typical samples, we can observe that RSO samples exhibits a sharp distribution and Typical samples have tails. The oxide thickness uniformity of RSO samples is better than that of Typical ones because the tunneling current is very sensitive to oxide thickness.Figure 4(a) and (b) show the C-V curves of RSO and Typical samples, respectively. The typical samples are actually more leaky. By examine the C-V curve in the depletion region, we can say RSO samples has less interface state densities than typical ones. Besides, their flat band voltages are almost the same. So the reduction of tunneling current of RSO samples is not due to the flat band voltage shift.

Figure5 shows the oxide thickness nonuniformity effect on tunneling current. If a local small region under a capacitor owns thinner oxide, the magnitude of tunneling current will increase dramatically. This can be used as a possible reason to explain the reduction in tunneling current in RSO samples since their oxide thickness uniformity is better. Figure5 tell us another possible reason that the more density of interface states, the larger of tunneling current. Other literature also support this inference.[2][3] The smaller interface states density of RSO samples also contributes to the reduction of it's tunneling current.

Figure7 shows the defect created on wafer in RST+O samples. It appears to be concentric circles in shape. These defects were not observed in Typical+O samples. The oxide thickness distribution of RST+O and Typical+O samples are shown in Fig.8. From Fig.8(a) we can observe three local thicker oxide region. This regions are just near the contact of wafer and three quartz pin holder. It is suggest that the huge thermal stress between silicon and quartz induced by RST will create many defects in silicon bulk and surface. So that the oxidation rate on the defect region will be enhanced. The RST+O sample has larger average thickness and thickness standard deviation than the Typical+O sample under the same following oxidation condition. The distribution of 1.2nm RST+O sample in Fig.9 seems to be normal. But that of 1.5nm and 1.8nm RST+O samples appear obvious increase in tunneling current magnitude and nonuniformity. Since the RST will create many defects and enhance the surface roughness, the behaviors of 1.5nm and 1.8nm RST+O samples are in expectation.

4. Conclusions

Ultra thin gate oxide (<2nm) with better reliability can be prepared by RSO technology with respect to conventional one and these new technology has relative low average process temperature. The reduction of tunneling current is not due to flat band voltage shift or electron trapping. Both simulation and experimental results indicate it is possible caused from the improvement in oxide thickness uniformity and the reduction of interface states density. However, the effect of RST before oxidation seems to affect oxide quality negatively. But by the study of RST, the thermal stress problem in RTP could be investigated more clearly.

Acknowledgments

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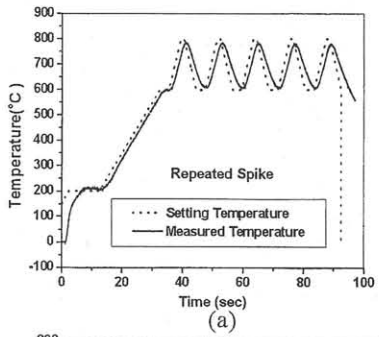
References

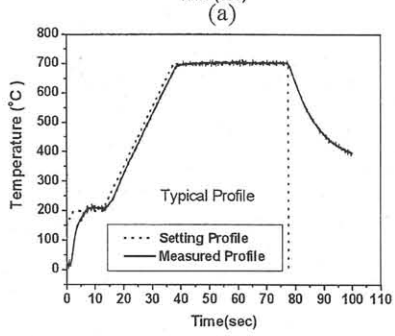
[1] Chao-Chi Hong, et al. IEEE Trans. on Semiconductor Manufacturing, Brief, to be published in August 2001.

[2] Mohamed Yehya Doghish and Fat Duen Ho, IEEE Trans. on Electron Device, **39**, p.2771, (1992).

[3] Chia-Hong Huang and Jenn-Gwo Hwu, Journal of Applied Physics, vol.89, p.5497,May, 2001.

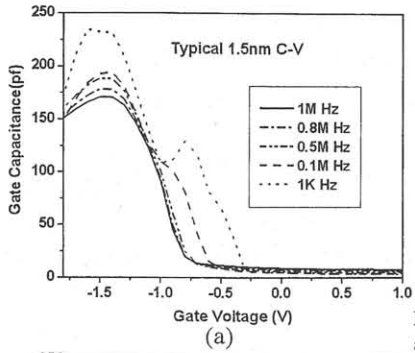


(a)

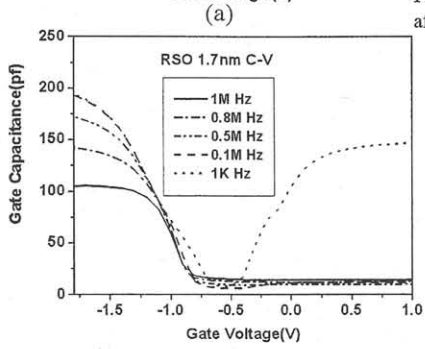


(b)

Figure1 The temperature setting and measured profiles for (a) repeated spike and (b) typical cases.



(a)



(b)

Figure4 The C-V curves for (a)Typical and (b) RSO samples in various frequency.

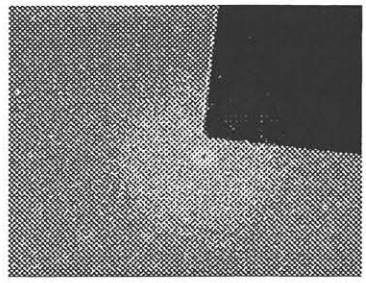
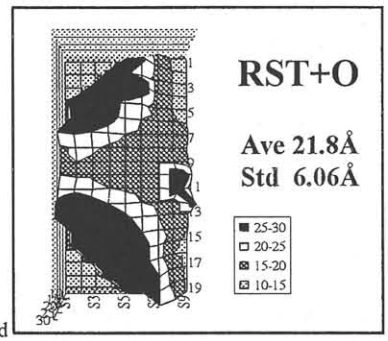


Figure7 The photograph of defects on wafer after RST+O process.



(a)

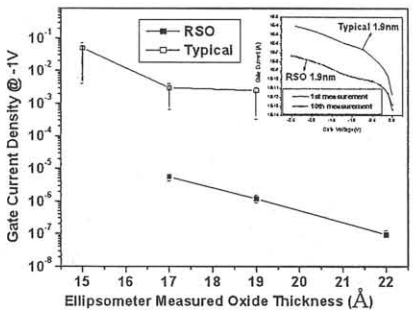


Figure2 The comparison of tunneling current density under –1V versus ellipsometer measured oxide thickness for RSO and Typical samples. The I-V curve of 1.9nm RSO and Typical samples in the 1st and the 10th measurements are shown in the inset,too.

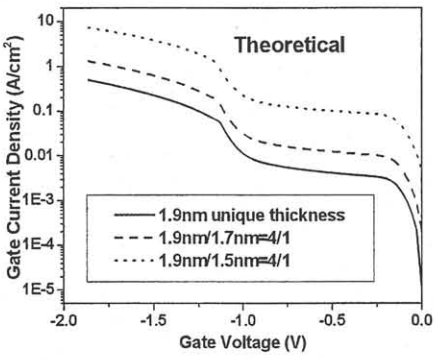
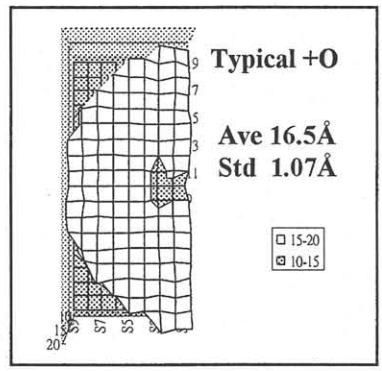


Figure5 The simulated result of local-thinning effect on the tunneling current.



(b)

Figure8 The oxide thickness distribution on a half 3-inch wafer for (a) RST+O and (b) Typical+O samples.

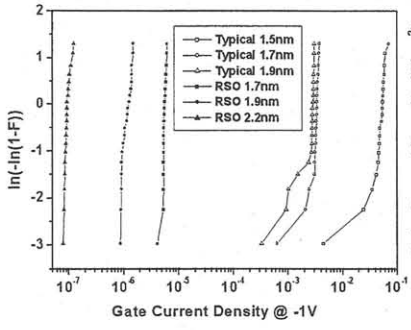


Figure3 Weibull plots of tunneling current density under –1V bias for RSO and Typical samples in various oxide thickness.

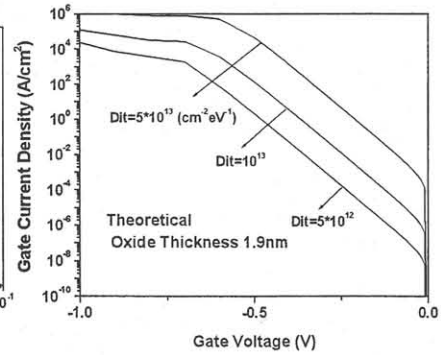


Figure6 The simulated result of interface states density effect on the tunneling current.

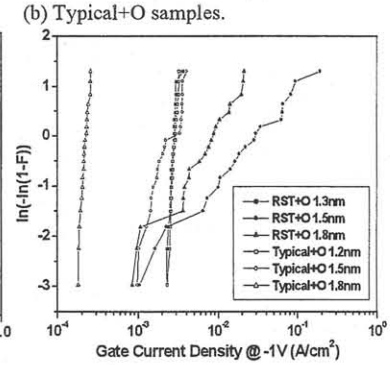


Figure9 Weibull plots of tunneling current density under –1V bias for RST+O and Typical+O samples in various oxide thickness.