

A-4-3

Improved Transconductance and Gate Insulator Integrity of MISFETs with Si₃N₄ Gate Dielectric Fabricated by Microwave-Excited High-Density Plasma at 400 °C

Ichiro Ohshima, Hiroyuki Shimada¹, Shin-ichi Nakao, Weitao Cheng, Yasuhiro Ono¹, Masaki Hirayama, Shigetoshi Sugawa, Herzl Aharoni^{2,3} and Tadahiro Ohmi²

Phone: +81-22-217-5564 Fax: +81-22-217-5551 e-mail: ohshima@sse.ecei.tohoku.ac.jp

Department of Electronic Engineering, Graduate School of Engineering, Tohoku University, Sendai 980-8579, Japan

¹New Device Development Group, SEIKO EPSON Corporation, Nagano 399-0293, Japan,

²New Industry Creation Hatchery Center, Tohoku University, Sendai 980-8579, Japan

³Department of Electrical and Computer Engineering, Ben-Gurion University of the Negev, Beer-Sheva 84105, Israel

FAX: +972-8-6472-949 email: Herzl@ee.bg.ac.il

Abstract

A low-resistivity metal gate Metal-Nitride-Semiconductor MNSFETs technology, exhibiting an excellent transconductance and high gate insulator integrity is reported. The gate stack consists of directly grown Silicon Nitride (Si₃N₄) film using microwave-excited (2.45GHz) high-density (<10¹²cm⁻³) Ar/N₂/H₂ or Ar/NH₃ plasma and Tantalum Nitride/bcc-phase Tantalum (~15μΩcm)/Tantalum Nitride, [TaNx/(bcc-Ta)/TaNx] stacked metal gate (<1.0ohm/sq).

Introduction

The scaling down of MOSFETs in ULSI Technology dictate a reduction in the gate Equivalent Oxide Thickness (EOT) down to the scaling limit, resulting an increase of the leakage current, due to direct tunneling, for Tox<3nm. Accordingly an effort is made to replace SiO₂ gates by higher dielectric-constant films, such as Si₃N₄ [1][2], ZrO₂ [3] and HfO₂ [4]. Another problem regards the undesirable increase in EOT, due to the influence of the polysilicon gate depletion layer capacitance. Accordingly, in order to avoid this problem, a metal gate is proposed as a solution.

We have already reported the attractiveness of Si₃N₄ as a high-K gate insulator, grown by using microwave-excited high-density plasma at 400°C [2], and of TaNx/(bcc-Ta)/TaNx stack as a metal gate electrode, due to its low resistivity [7]. Accordingly, they are used in this work. As a result, an excellent transconductance of Si₃N₄-MNSFETs as well as high gate insulator integrity, of TaNx gate MNS capacitors are reported.

Experimental

TaNx MNS capacitors and TaNx/(bcc-Ta)/TaNx stacked metal gate FDSOI-MNSFETs were fabricated (Fig.2). The Capacitors were fabricated on Cz phosphorus doped 0.8-1.2 Ω·cm, (100) silicon wafers and the SOI-MNSFETs were fabricated on SOI wafers (SOI/BOX=48nm/200nm). Si₃N₄ films were grown as the gate insulator in an Ar/N₂/H₂ (for FETs) or Ar/NH₃ (for capacitors) plasma system (Fig.1), at pressure ratios of 93/5/2 or 96/4, respectively, at 400°C. The applied microwave power density and frequency, were 5W/cm² and 2.45GHz, respectively. The three layers of the stacked TaNx/(bcc-Ta)/TaNx (=15nm/160nm/15nm) structure, were then successively deposited as a gate metal, by RF (40.68MHz, 80W) sputtering, at room temperature. S/D of FDSOI-MNSFETs was formed by ion-implantation (⁷⁵As⁺:15keV-1.5 × 10¹⁵cm⁻²) and post implantation annealing at 450°C for 5hours to activate the implanted dopants [8].

Results and Discussions

Fig.3 shows C-V characteristics of TaNx/(bcc-Ta)/TaNx metal gate MNS capacitor. Flat band voltage shift is below

4mV. Typical Id-Vg characteristics of the MNSFET are shown in Fig.4. In Fig.5 a comparison of the transconductances(g_m) of a MNSFET and a MOSFET both with stacked TaNx/(bcc-Ta)/TaNx metal gates, is shown. The transconductance of nMNSFET is higher than that of nMOSFET in the high Eox range. Similar result was obtained in JVD Si₃N₄ MNSFETs [9]. Fig.6 shows the combined reflected X-Ray intensity from the Si₃N₄ surface and Si₃N₄/Si interface as well as from the SiO₂ surface and SiO₂/Si interface, as a function of the incident X-Ray angle, measured by Grazing Incident X-Ray Reflectivity (GIXR)[10]. This measurement yield the interface roughness as summarized in Table I, showing that the interface roughness of the Si₃N₄/Si is smaller than that of SiO₂/Si. TEM cross section view of TaNx/Si₃N₄/Si and TaNx/SiO₂/Si structures are shown in Fig.7, which confirm that Si₃N₄/Si exhibit smoother interface. The findings of Table I and Fig.7 can explain the higher transconductance of MNSFET than that of MOSFET (Fig.5) by the smaller interface roughness [11]. Fig.8 and 9 show the charge to breakdown and the time to breakdown characteristics, respectively, for three Vg values, of TaNx gate MNS capacitors, which exhibit high integrity thin (2.44nm) Si₃N₄ gate insulator. Fig.10 was obtained from the 50% failure rate values of Fig.9. The 10 years lifetime was determined by extrapolation at Vg=2.55V for EOT=2.44nm Si₃N₄ films [12].

Conclusion

Metal-Nitride-Semiconductor MNSFETs technology is presented, exhibiting excellent transconductance and high gate-insulator integrity. The higher transconductance of the MNSFET with respect to that of MOSFET can be explained by the lower interface roughness.

Acknowledgements

The authors would like to thank Technos Co., Ltd. for GIXR measurement.

References

- [1] T.P Ma, IEEE T-ED, vol. 45, p.680 (1998)
- [2] K. Sekine, T. Ohmi et al., IEEE T-ED, vol. 47, no.7, p. 1370 (2000)
- [3] C.H. Lee et al., IEDM Tech., p.27 (2000)
- [4] L. Kang et al., IEDM Tech., p.35 (2000)
- [5] Hisayuki Shimada, T. Ohmi et al., IEDM, p. 881 (1995)
- [6] J. C. Hu et al., IEDM, p. 825 (1997)
- [7] Hiroyuki Shimada, T. Ohmi et al., SSDM, p. 460 (2000)
- [8] A. Nakada, T. Ohmi et al., J. Appl. Phys., vol. 81, p. 2560 (1997)
- [9] S. Mahapatra et al., VLSI Tech., p. 79 (1999)
- [10] S. Terada., ISSM, p.365(1999)
- [11] M. Takagi et al, IEDM, p. 575 (1998)
- [12] J.H. Stathis et al., IEDM, p.167 (1998)

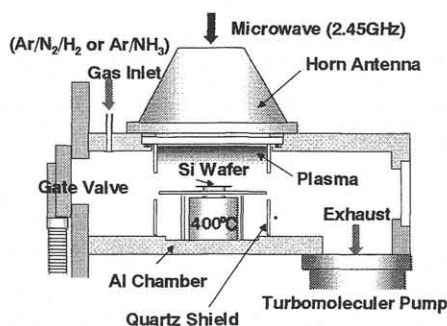


Fig.1 Microwave-excited high-density plasma system. Silicon nitride gate insulator is grown at 400°C.

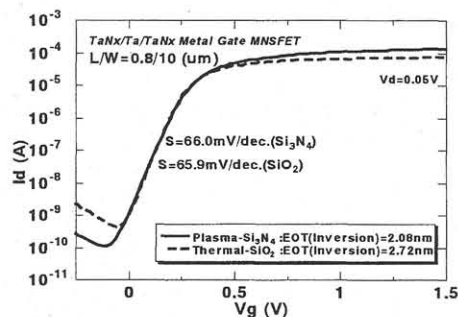
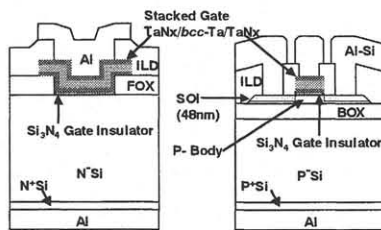


Fig.4 Id-Vg characteristics of TaNx/(bcc-Ta)/TaNx stacked metal gate FD-SOI nMNSFETs and nMOSFETs.



(a) Capacitors on Bulk wafer (b) FD-SOI nMNSFET
Fig.2 Cross sectional view of fabricated (a) capacitors and (b) FD-SOI nMNSFETs, both devices contain TaNx/(bcc-Ta)/TaNx stacked a metal gate. The top TaNx is introduced as a protective layer from oxidizing ambient.

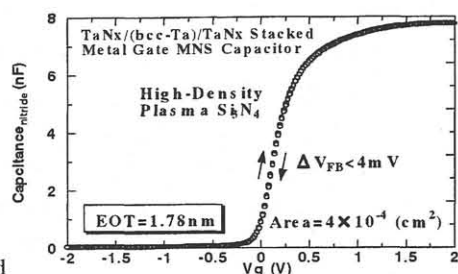


Fig.3 C-V characteristics of TaNx/(bcc-Ta)/TaNx stacked metal gate MNS capacitor.

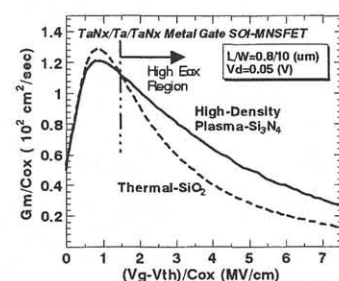


Fig.5 Comparison of transconductances ($V_d=0.05V$) of TaNx/(bcc-Ta)/TaNx stacked gate MNSFET and MOSFET.

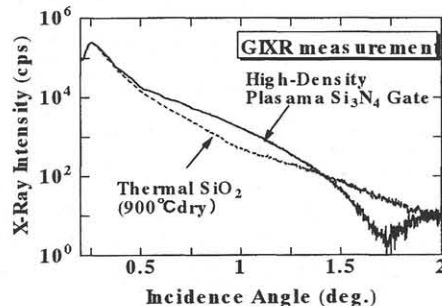
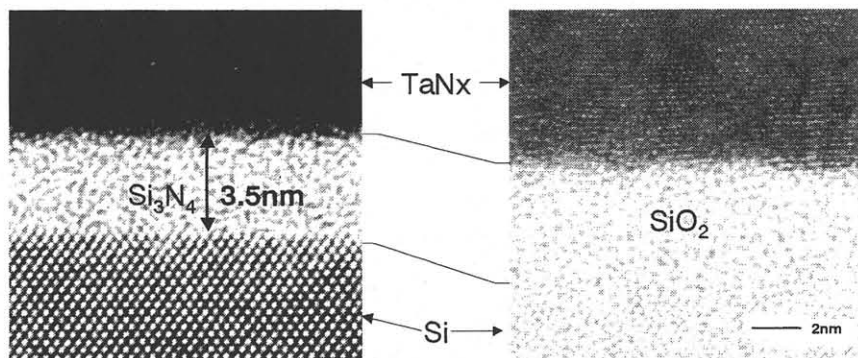


Fig.6 Combined X-Ray Intensity reflected from the surfaces of the respective insulating films and from their interfaces with the Si substrate.

Table I Interface roughness of the gate insulator/Si interface.

Gate Insulator/Si Interface	Interface Roughness
Si ₃ N ₄ /Si	Below Detection Limit (<0.1nm)
SiO ₂ /Si	0.29nm



(a) TaNx/Si₃N₄/Si

(b) TaNx/SiO₂/Si

Fig.7 TEM cross section view of (a) TaNx/Si₃N₄/Si and (b) TaNx/SiO₂/Si

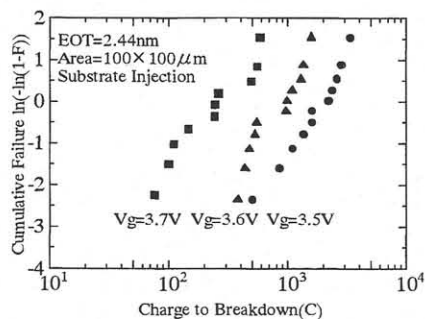


Fig.8 Charge to breakdown characteristics (Qbd) of PVD-TaNx gate MNS capacitors, for three V_g values.

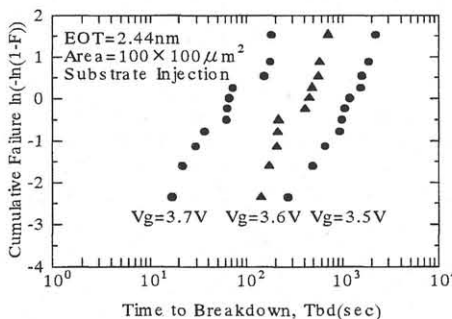


Fig.9 Time to breakdown characteristics (Tbd) of PVD-TaNx gate MNS capacitors, for three V_g values.

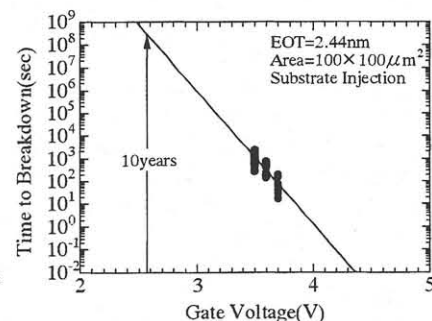


Fig.10 Lifetime extrapolation of a Si₃N₄ MIS capacitor, indicating 10 years lifetime for $V_g=2.55V$.