Extended Abstracts of the 2001 International Conference on Solid State Devices and Materials, Tokyo, 2001, pp. 186–187

A-6-1

Manufacturable 0.13 μm DRAM Technology for 512M DDR DRAM

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1. Introduction

We develop 0.13 μm DRAM technology for 512M DDR DRAM suited for 400 mil package. To improve the cell efficiency using the large mat size (512 row $\times$ 512 column), the low resistance polymetal (W/WNx/Poly-Si) gate and W bitline are adopted to reduce the RC delay time [1] and the TaON dielectric material is developed with the MIS capacitor structure to increase the cell capacitance. KrF lithography is extended to 0.13 μm DRAM technology with the optical techniques such as the full chip OPC, the critical layer PSM, and extreme OAI.

One of the blocking issues for the 0.13 μm DRAM technology is the characterization of the cell transistor. To obtain the reasonable characteristics, the careful treatment about the contact is important.

2. Key technologies

The process sequence for polymetal (W/WNx/ Poly-Si) gate is as follows: Shallow trench isolation (STI) is followed by shallow well and channel ion implantation. After 57 $\AA$ gate oxidation, 800 $\AA$ Poly-Si is deposited. And 50 $\AA$ WNx and 650 $\AA$ W are deposited by sputtering.

Because of the ILD1 gap fill issue, we apply the double spacer scheme. 250 $\AA$ nitride is deposited and NBN implant with tilt angle is applied. Then first spacer is fabricated and the second spacer of 150 $\AA$ nitride is deposited (fig. 1). Recently Saino et al. [3] show that the GIDL current impacts the tail distribution of refresh time. Fig. 2 shows the cell junction leakage current as the first spacer etch time. As the etch time is decreased, the GIDL current is decreased. Although the sub loss is only 10 $\sim$ 20 $\AA$ in 19 sec etch time, the effect on the GIDL current is enormous. The damage formed during the sub loss seems to role as the trap assisted tunneling center.

We use the bar type SAC scheme in the LPC for the sufficient overlay margin (fig. 3). Because the contact area at the bottom is small ($\sim 0.05\mu m \times 0.05\mu m$), the reduction of damage and removal of polymer residue by post etch cleaning are important for the good contact resistance. Fig. 4 shows the I_D-V_D curves with the gate voltage, 1.5V, 2.5V, and 3.5V. In the normal wet cleaning (a), the abnormal curves which are the characteristics of the high contact resistance [4] are occured, but the normal curves are appeared with the dry cleaning. In the small area contact the wet cleaning seems to have difficulty for curing the damage and removing the polymer residue.

The cumulative plots of the contact resistance as the cleaning split at the SNC and the SN are shown in fig. 5. The dry cleaning is also necessary for the uniformity improvement of the contact resistance. The isolation between the plugs is accomplished by the CMP process. Additional implant for the compensation of the dopant loss during the CMP process is needed for the contact resistance improvement.

We use the W bitline scheme with 0.09 μm linewidth which is obtained during the hardmask etch step. The hole type SAC scheme (fig. 6) are used in the SNC and the concern about the overlay margin is solved by the narrow bitline. Fig. 7 shows the cup type MIS capacitor structure with inner MPS. The capacitor dielectric, TaON, has the equivalent oxide thickness of 25 $\AA$. The measured capacitance and the leakage current are shown in fig. 8.

In BEOL processes, we use double metal interconnections, The bitline is used for the local interconnection and the metal layer is mainly used for the global interconnection.

3. Device integration result

The thermal position and temperature is very important to obtain the stable contact resistance of the cell. Fig. 9 (a) shows the cell contact resistance as RTP versus furnace anneal at the final step. The contact resistance is lowered about 20 % with the RTP than that with the furnace anneal. We obtain sufficient transistor performance by using a shallow junction and halo structure (fig. 9 (b)). The key technologes of 0.13 μm DRAM is summarized in Table. 1.

4. Conclusion and summary

We report the 0.13 μm DRAM technology for 512M DDR DRAM suited for the 400 mil package. The key process is polymetal (W/WNx/Poly-Si) gate, bar type LPC contact, W bitline, hole type SNC, and the MIS TaON capacitor. To obtain the good contact resistance in the cell, the dry cleaning is essential for all contacts, LPC, SNC, and SN. The careful thermal treatment is also necessary.

References

[1] J. W. Jung et al., IEDM, S15-5 (2000).
[2] W.S. Jeong et al., IEDM, S15-2 (2000).
[3] K. Saino et al., IEDM, S36-3 (2000).
[4] Y. H. Kim et al., KCS, 541 (2001)

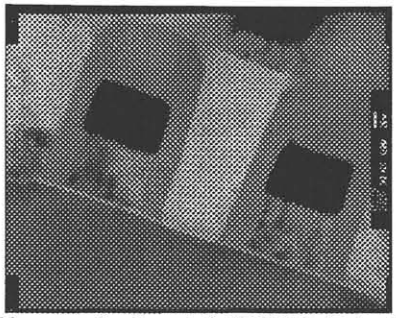

Fig. 1. TEM image of polymetal (W/WNx/Poly-Si) gate.

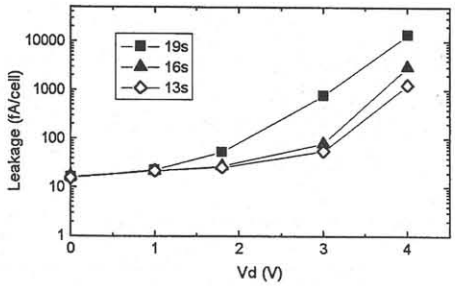

Fig.2. Cell junction leakage current as the first spacer etch time.

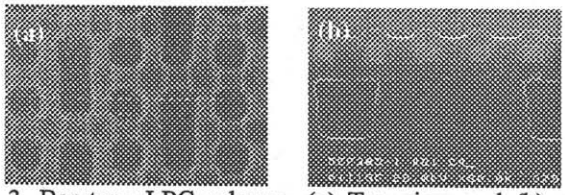

Fig. 3. Bar type LPC scheme. (a) Top view and (b) cross section.

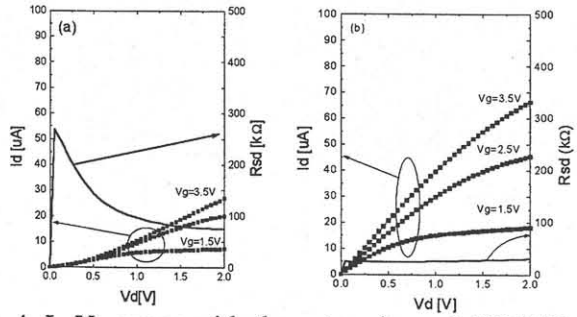

Fig. 4. I_D-V_D curves with the gate voltage, 1.5V, 2.5V, and 3.5V. (a) Wet cleaning and (b) dry cleaning.

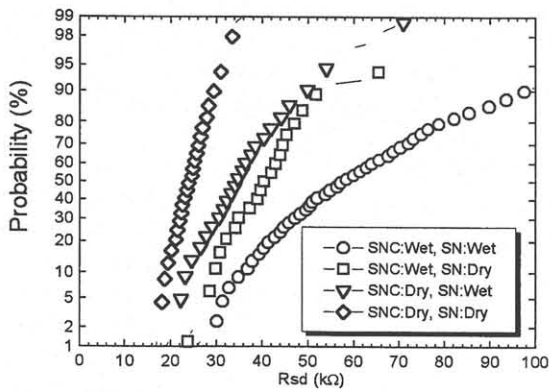

Fig. 5. Cumulative plots of the contact resistance as the cleaning split at the SNC and the SN.

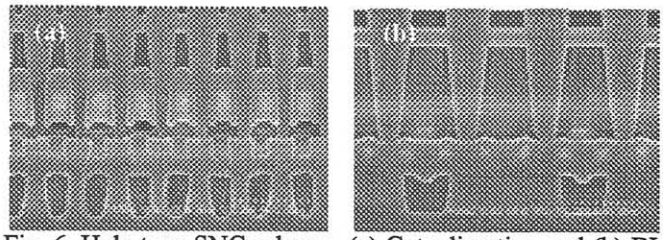

Fig. 6. Hole type SNC scheme. (a) Gate direction and (b) BL dieection.

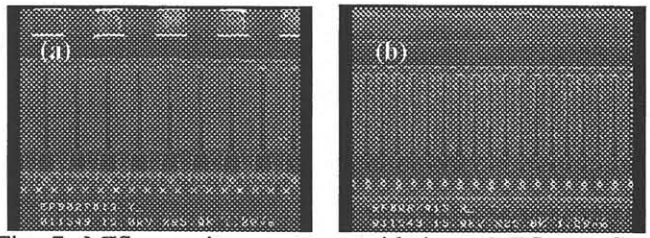

Fig. 7. MIS capacitor structure with inner MPS. (a) Gate direction and (b) BL direction.

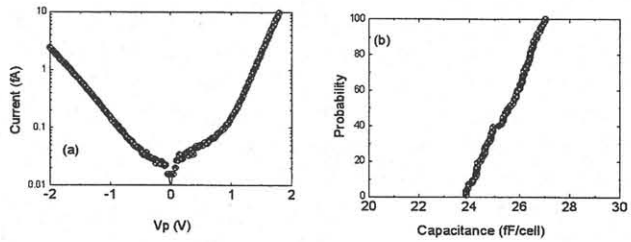

Fig. 8. TaON leakage current (a) and capacitance (b).

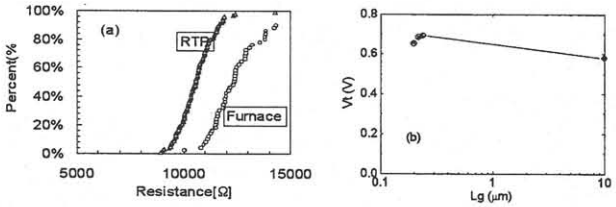

Fig. 9. (a) Cell contact resistance as RTP vs. furnace anneal. (b) Short channel characteristics of NMOS.

Technology	0.13 ㎛ DRAM Technology
Cell size	0.1352 ㎛^{2}
Vdd/Vcore	2.5V / 1.8V
I/O interface	SSTL-2
MAT size	512 row × 512 column
STI	0.25 ㎛ trench depth with HDP filling
Gate	Single gate polymetal (W/WNx/Poly-Si)
LPC	Bar type SAC
BL	W bitline
SNC	Hole type SAC
Capacitor	MIS-TaON (Inner cylinder)

Table 1. Key technologies for 0.13 ㎛ DRAM.