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A Technology for Suppressing Inter-Layer Dielectric Crack in a High Density DRAM

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1. Introduction

As the physical dimension shrinks, the thermo-mechanical stress becomes a hot issue in the process integration of a VLSI device. This stress frequently generates defects in the ILD (Inter Dielectric Layer), resulting in device failure [1]. Processes inducing abrupt temperature change, like RTA (Rapid Thermal Anneal) process, enhance the formation of defects and even produce significant crack propagation. This stress-induced-crack actually caused layer-short in the case of a high-density DRAM. In particular, the cracks were observed after RTA following contact plug implantation. In this work, process factors related to the stress-induced-crack formation have been investigated using a leading edge DRAM (1G bit DRAM) as a test vehicle. Stress simulation with various process conditions was also performed to understand the mechanism of the defect generation. Finally, a crack-free process with optimization of annealing and metallization processes for high density DRAM has been established.

2. Fabrication Process

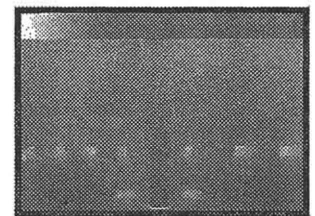
The main process flow is represented in Table I. Shallow trench isolation technology is utilized to satisfy deep sub-micron isolation scheme. W polycide capped with SiN layer is used as transistor gate stack, and W polycide bit line capped with SiN is then patterned after ILD deposition. After cell capacitor formation, planarization is performed by BPSG re-flow technology in order to form a smooth ILD transition profile between cell and peripheral areas. The vertical profile is shown in Fig. 1a. BPSG CMP process is also tested for the similar purpose. CMP process is rather complicated and shows poor uniformity compared to the etch-back process. After the ILD planarization, small contact opening is formed. Fig. 1b shows vertical structure after metal contact opening. Plug implantation is executed, followed by RTA (700 ℃, 20sec). In order to remove thin native oxide layer and some damaged layer, a dilute HF cleaning is carried out just prior to the barrier metal deposition. Self-Ion Plasma barrier metal (Ti/TiN), RTA, and CVD W deposition are followed sequentially.

3. Results and Discussions

We have reported that the cracks on the interfacial area between cell array and core region in the USG ILD scheme were due to stress mismatch by RTA after the barrier metal deposition [3]. These cracks were not observed in the BPSG ILD scheme with smooth transition profile between cell array and core region in the present study.

Table I. Main process flow for the Gigabit scaled DRAMs

Step	Process Flow
Isolation	Shallow Trench Isolation
Gate	W Polycide capped with SiN
Bit Line	W Polycide capped with SiN
Cell capacitor	Poly storage node +ono dielectric
Planarization	BPSG flow + Etchback
MC Hole Etch	High Density Plasma Etch
Plug	BF2, 30KeV, 1E15 + RTA
Metal	SIP Ti/TiN + RTA + CVD W E/B + Al reflow

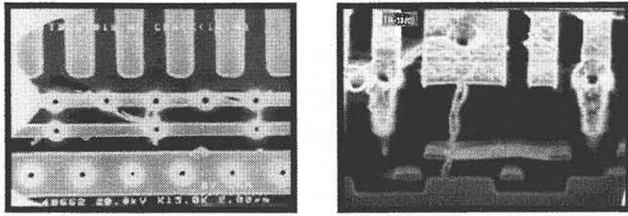


(a) BPSG etchback scheme (b) Metal contact profile

Fig. 1 Vertical structure with BPSG ILD

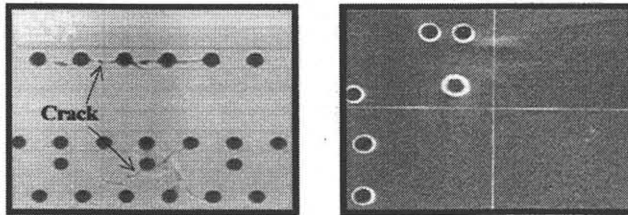
The block failure, however, was still observed and was disclosed as electrical shortening due to the ILD crack along the contact area. Fig. 2a and Fig. 2b represent the top view photograph and vertical profile of the failure point showing layer short due to the ILD cracks, respectively. According to our observation after each process steps, the ILD crack occurred during RTA performed after the plug implantation of metal contact. The effects of key parameters such as RTA temperature, layout, RTA step, and barrier metal thickness on the crack generation were investigated. It was found that the cracks were only generated when the RTA temperature was higher than 600°C, and initiated from metal contacts. Most of these cracks occurred in an area where the contact to contact space was close enough. The dense contact area with cracks and sparse contact area without cracks were represented in Fig. 3a, and Fig. 3b, respectively. It was also found that crack density increased when the rim of the contact opening had striations (Fig.4a). We believe that the

striations act as crack initiating sites and increase the crack density. Thus, proper dry etch technique was desired to suppress the formation of striation (Fig.4b).

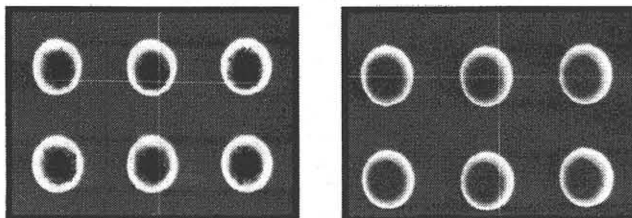


(a) Top view (b) Vertical SEM view
Fig. 2 Photographs to illustrate metal line shortage caused by ILD crack

These cracks were, however, not found when the RTA was applied after the barrier metal deposition. The block failure rates due to the crack according to various process conditions were represented in Fig. 5. These clearly show that the crack formation was mainly dependent on the RTA process executed before the barrier metal deposition, but independent of RTA applied after barrier metal deposition.

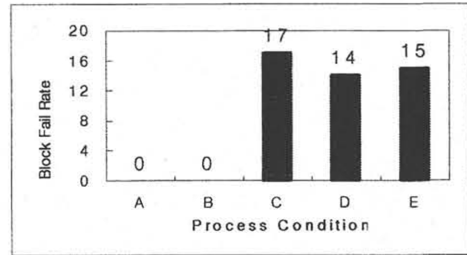


(a) Dense contact area with crack (b) Sparse contact area without crack
Fig. 3 Plain SEM images to show crack formation which depends on the contact density



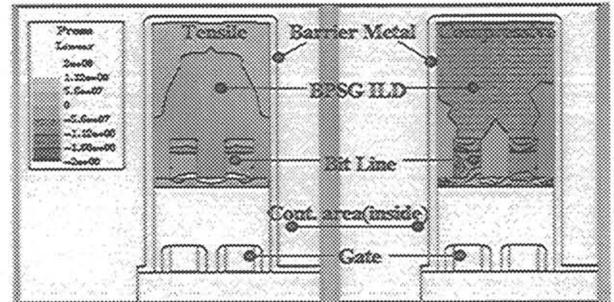
(a) With striation (b) Without striation
Fig. 4 Bird's eye views of contact profiles with and without striation

To find out the possible causality for this phenomenon, stress simulation was conducted using ABAQUS method [2]. Fig. 6a and 6b represent the results of stress simulation. These show that the RTA after barrier metal deposition produces more compressive stress on the ILD and less abrupt stress transition compared to the RTA before barrier metal deposition. As ILD crack is apt to be created under tensile stress and abrupt stress transition, compressive stress and relaxed stress transition prevent ILD layer from forming cracks. When RTA after the contact plug implantation was skipped, RTA after the barrier metal deposition plays a role of dopant activation as well as barrier metal stuffing [4]. In this case, RTA temperature after barrier metal deposition should be applied above 700℃ to attain stable contact resistance for the small size metal contact.



A	RTA-1 skip/Ti400Å/TiN600Å/RTA-2 700℃
B	RTA-1 skip/Ti400Å/TiN600Å/RTA-2 750℃
C	RTA-1 700℃/Ti400Å/TiN600Å/RTA-2 650℃
D	RTA-1 700℃/Ti400Å/TiN600Å/RTA-2 700℃
E	RTA-1 700℃/Ti400Å/TiN300Å/RTA-2 650℃
●	RTA-1: RTA before Barrier metal deposition
●	RTA-2: RTA after Barrier metal deposition

Fig. 5 Distributions of block failure with different process conditions



(a) RTA before barrier metal depo. (b) RTA after barrier metal depo.
Fig. 6 ILD stress simulation with two different processes near contact hole

4. Conclusions

The reliability of a DRAM was greatly influenced by contact forming process. BPSG ILD cracks across metal contacts were formed after the RTA process. The mechanism of crack formation was investigated using ABAQUS simulator. Tensile stress seems to be enhanced at the contact area during the rapid thermal change, resulting in crack formation. It was suppressed when the RTA was applied after the barrier metal deposition. To minimize the crack formation and attain low contact resistance, relatively high temperature RTA (≥700℃) process after barrier metal deposition was employed without RTA after the contact plug implantation. These results were well corresponding to the simulation results.

References

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