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Advanced Retrograde Well Technology for 90-nm-node Embedded SRAM by High-Energy Parallel Beam

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1. Introduction

Continuing efforts have been devoted to down scale LSI to improve the circuit performance and to reduce the chip cost. In constructing SoC (system on a chip), a demand for ultra high-density embedded SRAM is rising as a replacement for embedded DRAM, since SRAM process is highly compatible with LOGIC process. For miniaturization of CMOS devices, shrinkage of the inter-well isolation is significant. Especially the reduction in the n^+–p^+ spacing has large impact on SRAM. The dependence of the SRAM memory cell size on the n^+–p^+ spacing is illustratively estimated in Fig. 1. Shrinking the n^+–p^+ spacing is one of the key issues for scaling the SRAM cell size down to sub-1 μm^2 in 90-nm node.

Retrograde well using high-energy ion-implantation is widely used for CMOS devices [1]. High-energy ion-implantation is usually done with the tilt angle around 7° to avoid channeling. This is because channeling ion-implantation causes spatial variation within a wafer, since a conventional batch-type implanter has small variation in the tilt angle across the wafer [2]. Tilted implantation, however, results in the skew of the well boundary due to the encroachment of deep implantation and the shadowing by thick photoresist [3]. This skew of the well boundary imposes a limit on inter-well isolation and small tilt angle implantation is needed to break through the limit. In this paper, we have studied the application of high-energy parallel beam by a single-wafer implanter to retrograde well. Feasibility of small or zero tilt angle implantation by high-energy parallel beam is discussed, and its necessity for the inter-well isolation of 90-nm-node embedded SRAM is demonstrated.

2. Results and Discussion

Fig. 2 schematically shows the skew of well boundary caused by tilted implantation. The effects of this skew on the inter-well isolation characteristics is clearly shown in Fig. 3. In Fig. 3, sub-half-micron retrograde well process is used to make matters clear. Minimum width between n^+/p^+ diffusion and the well boundary is determined by the spacing at which the breakdown voltage degrades to 10 volts. Each measurement point is fitted by a sinusoidal curve for an eye-guide; note that the sinusoidal curve for n^+–n-well spacing has reverse phase compared with that for p^+–p-well spacing. In device design, the margin between the diffusion and the well boundary should be set against the worst configuration, since it is practically impossible to limit their direction in a chip. To reduce the amplitude of the sinusoidal curve and improve the inter-well isolation, small tilt angle implantation should be needed.

Fig. 4 shows the sheet resistance and its uniformity within an 8-inch wafer for a conventional batch-type implanter and a single-wafer parallel beam implanter. The sheet resistance reduces with the reduction in the tilt angle since the profile spreads due to the channelling. The batch-type implanter gives poor uniformity for the small tilt angle, while parallel beam gives quit uniform doping profile regardless of the tilt angle. The parallel beam produces almost the same doping profile within a wafer even for 0°-channelling-implantation as shown in the SIMS profiles of Fig. 5.

Fig. 6 shows the results of the application of small tilt angle implantation to sub-half-micron retrograde well process. On average, the conventional batch-type implanter and the parallel beam implanter give almost the same dependence of n^+–n-well isolation characteristics on the tilt angle; except that the parallel beam is superior at 0°. This is because the variation in the tilt angle of the batch-type implanter causes only deterioration to the isolation characteristics at 0°. In Fig. 7, contour maps of the sheet resistance of n-well and the breakdown voltage of n^+–n-well which has 0.6-μm spacing are shown. The parallel beam gives no notable distribution both in the resistance and the breakdown voltage. Note that the variation in the breakdown voltage includes variations of other process such as lithography or the thickness of the field oxide film. Both of the maps of the batch-type implanter show larger variation, and the variation of the tilt angle in the wafer is reflected in the distributions both of the sheet resistance and the breakdown voltage. It should be noted that these variations of a batch-type implanter are hardly improved by the rotational or multistep implant. Parallelism is quite important in small tilt angle implantation.

In Fig. 8, small-angle high-energy parallel beam is applied to 0.15-μm retrograde well process. Though the margin between the source-drain diffusion and the well boundary might be set according to operation voltage, it can be seen that 0°-implantation improves punchthrough resistance and the n^+-p^+ spacing can be shrunk by ~0.16 μm compared with the conventional 7°-implantation, which brings ~15% reduction in the SRAM cell size. Finally the impact of tilted implantation on MOSFETs near the well boundary is investigated by simulation. Fig. 9 illustrates 3-D simulation on the threshold voltage (V_{th}) for NMOSFETs formed around well boundary. Variation of V_{th} should be considered especially for high-density SRAM, since the variation is much significant for MOSFETs with narrow channel width and is irrespective of operating voltage. In the case of 7°-tilted implantation, the channel region of MOSFET should be 0.2-μm apart from well boundary to avoid the variation of V_{th}, while V_{th} does not vary down to 0.1-μm, in the case of 0°-implantation. In this aspect, small tilt angle implantation is indispensable for 90-nm-node high-density SRAM.

3. Conclusions

Advantage of retrograde well using high-energy parallel beam has been experimentally clarified for the first time. Conventional batch-type implanter requires tilted implantation to suppress the spatial variation in a wafer. Tilted implantation, however, imposes a limit on inter-well isolation, since it deteriorates the punchthrough resistance between source-drain diffusion and well, and causes the variation in threshold voltage for MOSFETs around well boundary. Parallel beam by a single-wafer implanter is found to give quite uniform doping profile even for 0°-normal implantation. Small tilt angle implantation by high-energy parallel beam improves inter-well isolation by ~0.16 μm compared with the conventional 7°-tilted implantation, which brings ~15% reduction in the SRAM cell size. This advanced retrograde well technology is indispensable for inter-well isolation of 90-nm-node embedded SRAM with sub-1-μm^2 cell.

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References

[1] T. Yamashita et al., IEDM Tech. Dig. (1997), p. 673.
[2] D. Kapila et al., IEEE Trans. on Semiconductor Man. Vol. 12, No. 4 (1999), p. 457.
[3] P. Gilbert et al., SPIE Vol. 3212 (1997), p. 228.

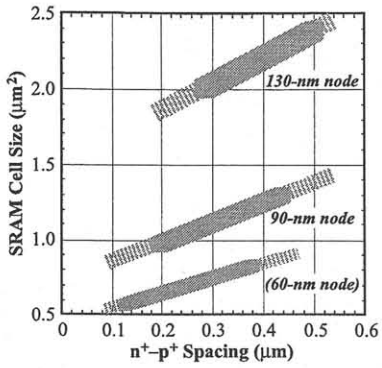


Fig. 1. Dependence of SRAM cell size on n^+–p^+ spacing.

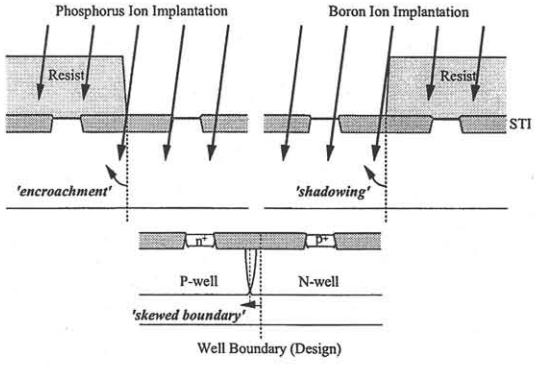


Fig. 2. Skew of well boundary caused by tilted implantation.

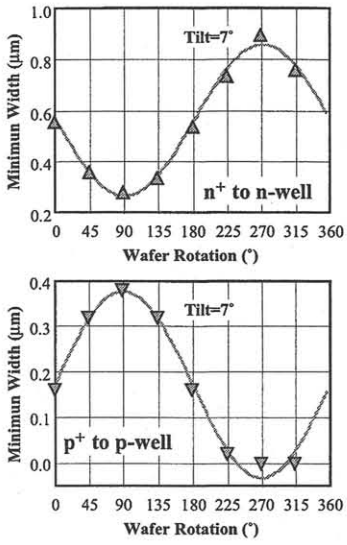
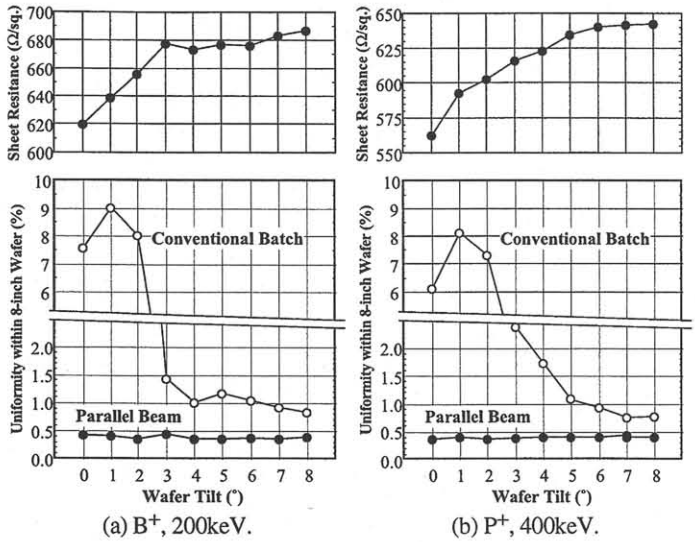
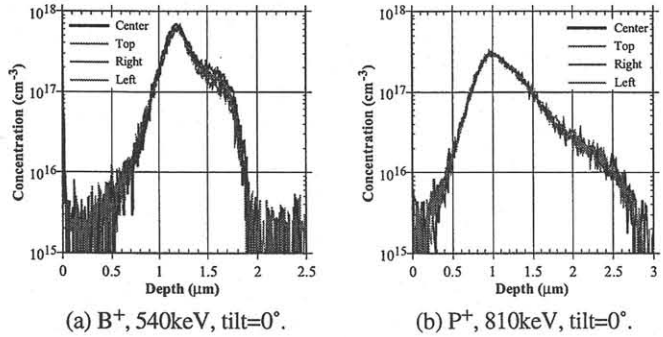


Fig. 3. Dependence of minimum spacing between well and source-drain diffusion on wafer rotation for 7°-tilted implantation.



(a) B^+, 200keV. (b) P^+, 400keV.

Fig. 4(a)-(b). Sheet resistance and its uniformity within 8-inch Wafer (after 900°C annealing).



(a) B^+, 540keV, tilt=0°. (b) P^+, 810keV, tilt=0°.

Fig. 5(a)-(b). SIMS profile of parallel beam.

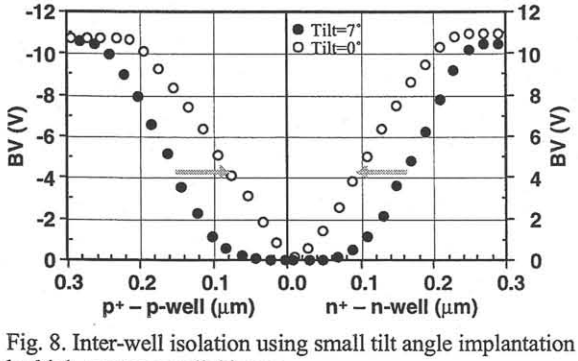
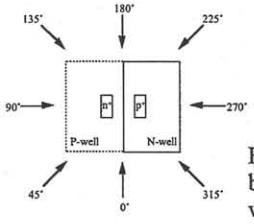


Fig. 8. Inter-well isolation using small tilt angle implantation by high-energy parallel beam.



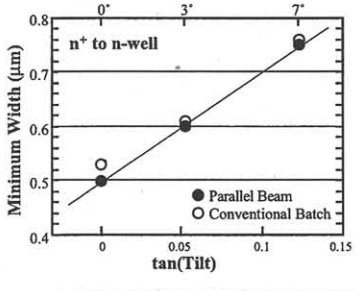


Fig. 6. Dependence of minimum spacing between n^+ and n-well on tilt angle.

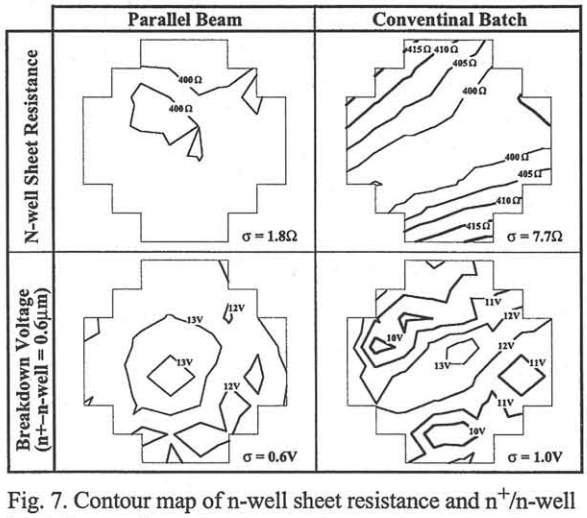
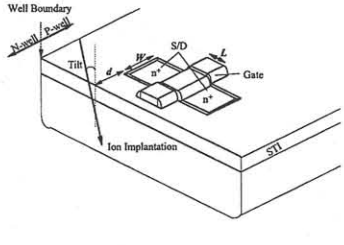


Fig. 7. Contour map of n-well sheet resistance and n^+/n-well breakdown voltage.



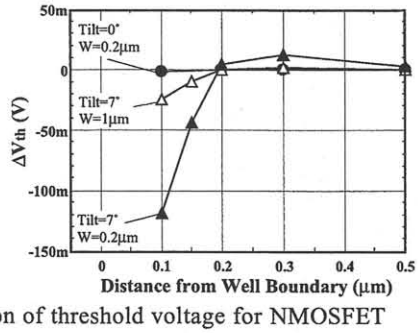


Fig. 9. Simulation on variation of threshold voltage for NMOSFET around well boundary.