Extended Abstracts of the 2001 International Conference on Solid State Devices and Materials, Tokyo, 2001, pp. 194–195

A-6-6

New STI Scheme to Compensate Gate Oxide Thinning at STI Corner Edge for the Devices Using Thick Dual Gate Oxide

Seong-Ho Kim, Sung-Hoan Kim, Sung-Eun Kim, Myung-Soo Kim, Joo-Han Park, and Eun-Soo Kim

LDI Process Architecture, LSI Development Team, System-LSI Division, Samsung Electronics Co., Ltd.
San#24, Nongseo-Lee, Kiheung-Eup, Yongin-Si, Kyungki-Do, 449-900, Korea
Phone:+82-31-209-6269, FAX:+82-31-209-6535, E-mail: gojira@samsung.co.kr, gojira@kist.re.kr

Abstract

This paper describes the results of designing a Shallow Trench Isolation (STI) process and a dual gate oxide method for overcoming a gate oxide thinning at STI corner edge, when dual gate oxides are used in one chip. Even though the pronounced difference of thickness exists between a thin (~40Å) and a thick gate oxide (~320 Å), we can obtain a good electrical characteristics by the prevention of a gate oxide thinning and a deep dent profile.

1. Introduction

It is generally known that Dual Gate OXides (DGOX) are used for realizing a low voltage (LV) and a high voltage (HV) operating part in one device. When a wet-etch back process is carried out for realizing the DGOX with STI, it can be considered that a Gate OXide (GOX) thinning is so severe at the edge of trench [1]. In this work, the thickness of thick GOX in a HV part is designed to be 320 Å, whereas that of thin GOX is 40 Å. When conventional STI and DGOX processes are adopted, we can observe a GOX thinning and the deteriorated edge profile of STI (so-called a dent) in our previous work. In order to resolve this problem, a Self-Aligned STI (SA-STI) may be considered. However, since this process is normally performed after the patterning of gate poly, SA-STI process is a complicated method and also has a miss-align issue between implantation steps and an active area [2]. In this work, we propose a new STI and a DGOX process to eliminate these problems.

2. Experimental

Dual gate oxide process for new STI scheme

In the conventional DGOX process, a thick GOX is simultaneously grown in both LV and HV parts and a photolithography process is followed. After the photolithography process, the thick gate oxide is removed using a wet etch-back and then a thin gate oxide is re-grown in a LV part. During this wet etch-back process, the degree of dent at STI corner edge increases. And this may be considered to cause the V_g-I_d hump characteristics of MOSFETs, as generally known.

Fig. 1 schematically describes the selected process steps to realize the DGOX in this study. After filling the trench of STI and Chemically Mechanically Polishing (CMP), the CVD Si_3N_4 and SiO_2 layers are deposited, and then a photolithography process is performed to remove the SiO_2 and Si_3N_4 layers in a HV part. The 450Å thickness of thick gate oxide is only grown in HV. When the SiO_2 and Si_3N_4 layers are etched in LV, the 450Å of GOX is reduced to about 320Å. After growing GOX in LV, we can acquire the minimum degree of dent at STI corner (Fig. 2). Therefore, this process can allow us to prevent the subthreshold double hump characteristics in a LV part by improving the edge profile of trench (Fig. 3).

SiN pull-back STI process

Although the DGOX process has many advantages in avoiding the recess of STI corner edge in LV, the GOX thinning problem still remains in HV. In this study, we suggest a new STI process scheme combined a SiN pull-back with a buffer oxide process in order to remove these effects.

Fig. 4 shows the schematic diagrams of the STI process used in this study. After trench etching, a SiN layer pull-back is carried out by a wet etch-back. A sidewall oxide is grown, and then a SiN liner is deposited on trench. In this time, the thickness of the sidewall oxide (S/O) has been varied in the range from 110Å to 500Å.

Fig. 5 shows the profile of trench, after the filling of trench and CMP. It can be observed that the thick buffered oxide (S/O) formed at the top edge of trench during S/O process. The SiN pull-back make possible to grow the buffered oxide (S/O) at STI corner edge, properly. However, it can be also supposed that the active area decreases with increasing the quantity of SiN pull-back. Consequently, the key technology of this process is determined by the thickness of the buffer oxide (S/O) and the quantity of SiN pull-back.

2. Results and discussion

Fig. 6 shows V_g-I_d characteristics for 2.5-μm width and 1.2-μm length with increasing substrate biases, when a conventional STI process is applied. It can be observed that the double subthreshold hump severely occurs. This extreme result indicates that the GOX thinning and/or the dent can exist at STI corner edge, as shown in Fig. 7. The thickness of GOX at STI corner edge is 79 Å, comparing that of an active area about 340Å. Also, the dent exists in the level of 150Å. In order to analyze this phenomenon, a stress simulation is carried out by TSUPREME IV (Fig. 8). From the simulation results, the compressive and the tensile stress are concentrated at STI corner edge, whereas only tensile stress prevails in active area. It is considered that this stress distribution affects the GOX thinning phenomenon, as previously reported [3].

Fig. 9 shows the STI corner edge profile, when the 300Å of buffer oxide (S/O) is grown. It is found that the growth of buffer oxide prevents the GOX thinning. This result suggests that the role of buffer oxide (S/O) is a dominant factor to control the GOX thinning. However, if the

thickness of buffer oxide (S/O) is thicker than 300 Å, it is likely to introduce a junction leakage current (N+/P-sub or P+/N-sub), due to the concentration of stress [4]. Fig. 10 shows V_g-I_d characteristics for 2.5-μm width and 1.2-μm length, when the thickness of buffered layer is 300Å. The double subthreshold characteristics is not observed in spite of increasing the substrate bias. From the result, the optimized thickness of buffer oxide (S/O) is determined to be 300 Å. In addition, the qualities of GOX with different processes are shown in Fig.11.

4. Conclusion

In this study, we describe a new process scheme to prevent the GOX thinning and the dent at STI corner edge using the SiN hard mask and modified STI process. When a new STI process is used, we can successfully resolve the double hump characteristics of MOSFETs in both LV and HV parts.

Acknowledgements

The authors would like to thank Dr. Jin-Tae Kim and Dr. Kang-Nyung Lee in Samsung Electronics Co. for their continuous encouragement and support.

References

[1] Y. Takeuchi, K. Shimizu, K. Narita, E. Kamiya, T. Yaegashi, K. Amemiya, and S. Aritome, *1998 Symposium on VLSI Technology Digest of Technical Papers* (1998) p. 102.

[2] S. Aritome, S. Satoh, T. Maruyama, S. Shuto, G. J. Hemink, R. Shirota, S. Watanabe and F. Masuoka, *International Electron Devices Meeting, 1994. Technical Digest* (1994) p. 61.

[3] P. Sutardja, W. G. Oldham, and D. B. Kao, *International Electron Devices Meeting, Technical Digest 1987* (1987) p. 264.

[4] S.-H. Pyi, I. S. Yeo, D.-H. Weon, Y.-B. Kim H.-S. Kim, and S.-K. Lee, IEEE Electron Device Letters, **20**, 384 (1999).

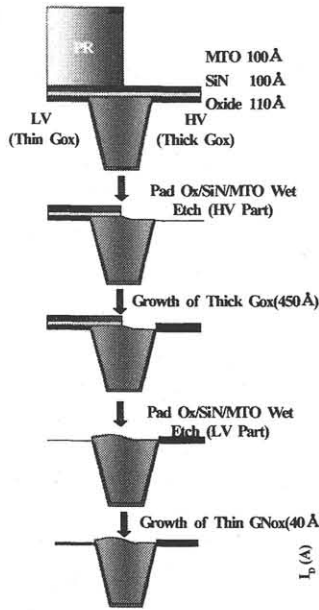

Fig. 1. Schematic diagram of a new DGOX process in this study.

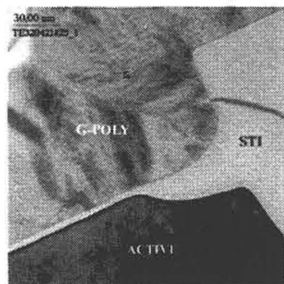

Fig. 2. Cross sectional TEM micrograph of final STI edge profile in LV part using a new DGOX process. (The thickness of S/O: 110 Å)

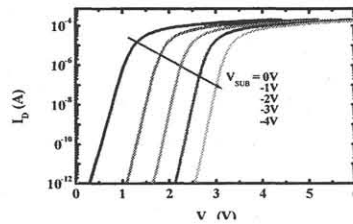

Fig. 3. Subthreshold characteristics of LV NMOS part using a new DGOX process.

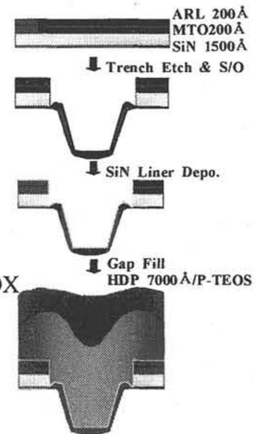

Fig. 4. Schematic diagram of a modified STI process.

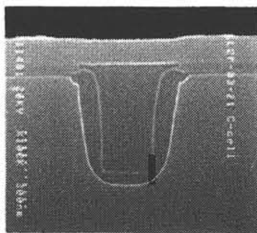

Fig. 5. Cross sectional SEM micrographs of STI profile with SiN pull-back. (The thickness of S/O: 500 Å)

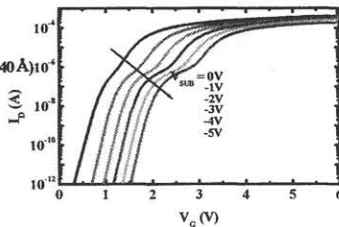

Fig. 6. Subthreshold characteristics of HV NMOS with 110 Å S/O thickness. (W/L = 2.5/1.2μm)

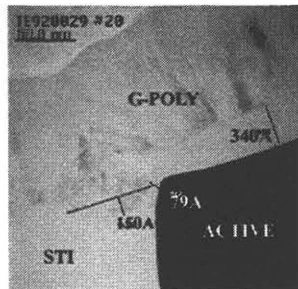

Fig. 7. Cross sectional TEM micrograph of final STI profile w/o SiN pull-back. (The thickness of S/O: 110 Å)

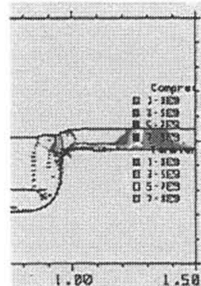

Fig. 8. The simulation result of stress distribution in STI corner edge with the growths of S/O, 500 Å and GOX, 500 Å.

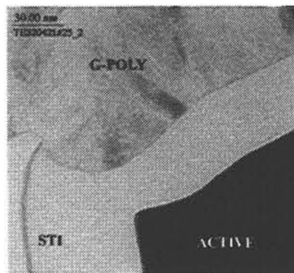

Fig. 9. Cross sectional TEM micrograph of STI corner edge profile with SiN pull-back. (Thickness of S/O: 300 Å)

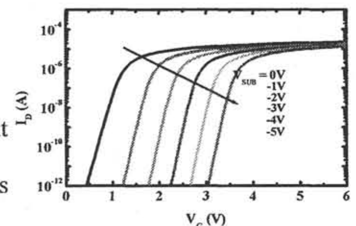

Fig. 10. Subthreshold characteri-stics of HV NMOS with 300 Å S/O thickness. (W/L = 2.5/1.2μm)

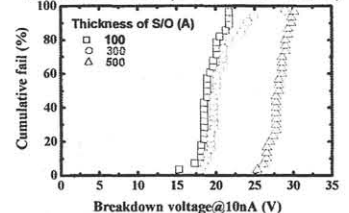

Fig. 11. Cumulative fail trends of GOX at field type pattern of HV NMOS with the different thickness of S/O.