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Three-Dimensional Integration of Fully Depleted SOI Devices

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1. Introduction

Recently, three-dimensional (3D) integration technology has attracted much attention since it offers the possibility of solving the serious interconnection problems in future LSIs. To realize high-performance and highly parallel processing LSIs, we have developed a new 3D integration technology using a novel wafer level stacking technique. We fabricated 3D stacked image sensor and 3D shared memory by stacking bulk device wafers [1-2].

However, one of the major concerns in such 3D LSI with bulk devices is an increase of total power consumption. Then, we tried to fabricate 3D LSI by stacking fully depleted SOI device wafers in order to reduce the power consumption. Fully depleted SOI devices are very useful to reduce the power consumption and to increase the speed. Furthermore, 3D LSI with SOI devices allow us to dramatically reduce the length of vertical interconnections which electrically connect an upper layer and a lower layer. This also leads to the decrease of the power consumption in addition to the increase of speed. In this paper, we describe a new 3D integration technology using fully depleted SOI device wafers.

2. New 3D Integration Technology Using SOI Wafers

The cross-sectional view of 3D LSI with SOI devices (SOI-based 3D LSI) is shown in Fig. 1. Key technologies developed for 3D LSI with bulk devices (bulk-based 3D LSI), such as formation of micro-bumps, wafer alignment and wafer bonding, were applied to realize such SOI-based 3D LSI. However, the mechanical wafer thinning method such as a mechanical grinding and CMP which can be employed to the fabrication of bulk-based 3D LSI cannot be applied to thin SOI wafer because this method causes the degradation of the device characteristics. Then, we examined to use dry etching and wet etching for thinning SOI wafer after stacking it. The fabrication sequence for SOI-based 3D LSI is shown in Fig. 2. After the device fabrication(Fig.2 (a)), In/Au micro-bumps were formed on metal wirings (Fig.2 (b)). The two wafers were face-to-face bonded through micro-bumps. After that, the liquid epoxy adhesive was injected into the gap between two wafers in a vacuum chamber to reinforce the bondability (Fig.2 (c)). Then, the upper wafer was thinned from the backside to exposure the buried oxide (BOX) using two kinds of methods. SF_6 gas and TMAH (Tetra-Methyl-Ammoium-Hydrooxide) were used for dry etching and wet etching, respectively, in a wafer thinning process to remove the Si substrate of upper SOI wafer (Fig.2 (d)). The BOX was used as a Si etch stop. Fig.3 shows the photomicrographs of SOI-based 3D LSI test chip. Fig.3 (a) and (b) show the photomicrographs of MOSFETs in lower and upper layers, respectively. Vias were formed through the BOX layer to expose the metal pads on the frontside of the upper layer and the metal wirings was formed to connect the metal pads on BOX layer (Fig.2 (e)). By repeating these process steps, SOI-based 3D LSI can be fabricated. Fig. 4 shows an SEM cross-sectional view of 3D LSI test chip with two device layers. It is clearly observed that two wafer layers are face-to-face bonded through the micro-bumps and the insulating epoxy adhesive and fully depleted SOI devices with SOI film thickness of 50nm are formed in both layers.

3.Result and Discussion

Fig.5 shows the subthreshold characteristic of nMOSFET with the gate length of 1.5 μ m in the lower layer before stacking (2D LSI) and after stacking (3D LSI). The device characteristic of nMOSFET in the lower layer was measured through the metal micro-bumps to electrically connect the upper wafer with lower wafer. As is obvious in Fig.5, the subthreshold characteristic of nMOSFET in the lower layer is not degraded even after staking. Fig.6 shows the subthreshould characteristics of nMOSFETs in SOI-based 3D LSI test chip. When the Si substrate of upper SOI device wafer was removed by plasma etching using SF_6 gas, the subthreshold characteristic of nMOSFETs in the upper layer is significantly degraded as shown in Fig.6 (a). Meanwhile, when it was removed by wet etching using TMAH, the degradation of subthreshold characteristic is less as shown in Fig.6 (b). It will be possible to further reduce the degradation by a careful surface cleaning and by the formation of the passivation film on the BOX layer after removing the Si substrate.

4.Conclusion

We developed a new SOI-based three-dimensional integration technology. We fabricated the SOI-based 3D LSI test chip with two layers and evaluated the basic characteristic of fully depleted SOI-MOSFET in this test chip. We demonstrated that the device degradation can be minimized by employing wet etching instead of plasma etching for removing the Si substrate of upper SOI wafer.

Acknowledgment

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References

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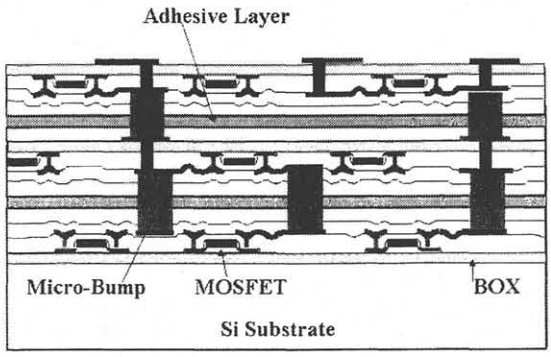


Fig.1 Cross-sectional structure of 3D stacked chip.

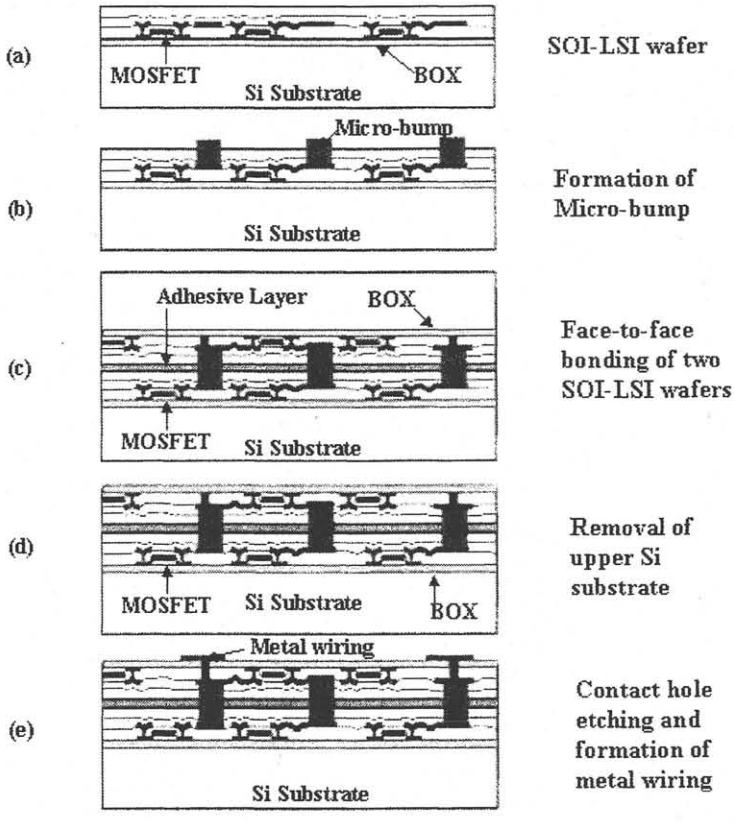
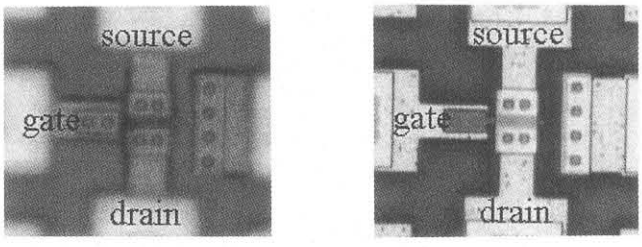


Fig.2 Fabrication process sequence.



(a) Lower layer (b) Upper layer

Fig.3 Photomicrographs of 3D stacked test chip.

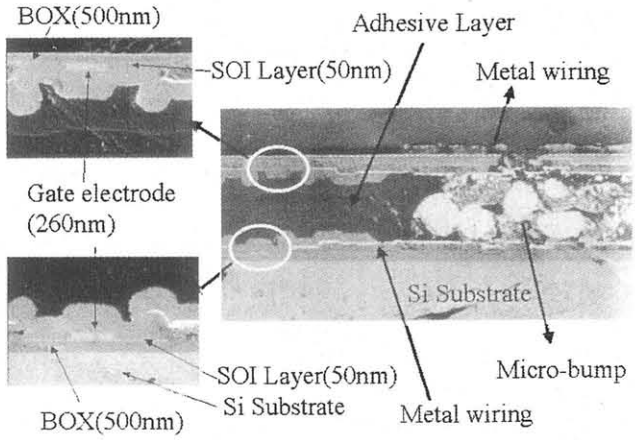


Fig.4 SEM cross-sectional view of 3D LSI.

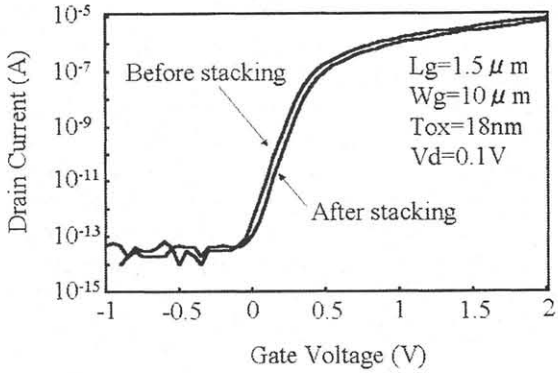
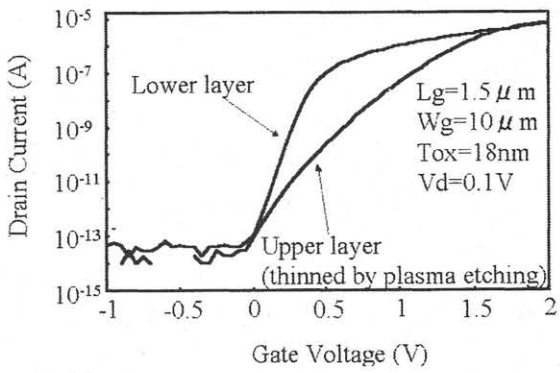
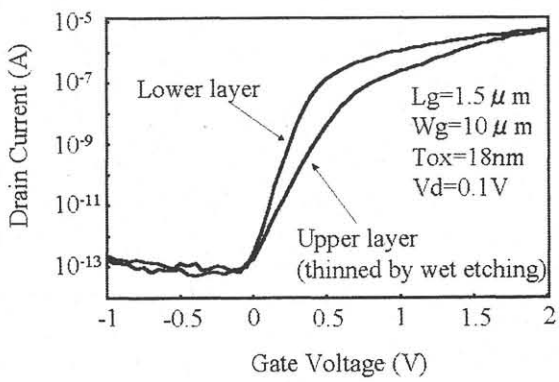


Fig.5 Subthreshold characteristic of nMOSFETs in the lower layer before and after stacking



(a) Thinning of upper layer by plasma etching.



(b) Thinning of upper layer by wet etching.

Fig.6 Subthreshold characteristics of stacked nMOSFETs.