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Feasibility of Direct Bonding Between CMP-Cu Films at Room Temperature for Bumpless Interconnect

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1. Introduction

As the trend of microelectronic systems move towards higher performance and speed, ultra-high density integration technology must be developed. Recently, the design concept named 'System on a Chip (SoC)' has come into vogue. However according to the numbers of devices and systems to be integrated on one chip keep growing, various problems are coming up for SoC such as mixed technical requirement, legal problem, higher development cost [1]. A possible solution for system level packaging is borderless coexistence of SoC and 'System on a Package (SoP)' [2]. Nevertheless, since the transmission delay in SoP is more serious than in SoC, it is inevitable that ultra-high density interconnect technology for SoP is developed. Concretely, the ideal bonding pitch is considered to be less than 10 μm, which can be a match for global interconnections on LSI chip.

However, there are other challenging problems at pitches below 10μm. Unlike conventional bump bonding, micro bumps used in ultra-high density interconnect can not contribute to reduce the thermal stress between two chips because enough self-deformation of bumps can not be expected. The solution for it is the combination of a thin chip and a thin substrate with no-bump structure or bumps with very low profiles, which we propose as *bumpless interconnect* [3]. Bumpless interconnect is unique in its construction, where two layer structures with Cu interconnections and insulators are bonded at the same plane as shown in Fig. 1. By applying this structure to interconnection between wiring layer and device layer, signal transmission rate will be improved dramatically because of the shortened distance between devices.

No ordinary bonding method that is carried out at elevated temperature may be applied for such interconnect structure because of the difficulties in high-accuracy alignment and supplying contact materials exactly. Surface activated bonding method (SAB) is based on the adhesive force across two atomically clean solid surfaces in contact, so there is no dependence on heat and interconnections can be obtained at room temperature. The clean surfaces with no oxidation layer are generated by Ar fast atom beam bombardment (FAB) of about 1.5 kV and 15 mA power source in high vacuum condition.

Another important requirement for bumpless interconnect is the highly flattened surface of Cu because large initial contact area is needed for SAB to ensure enough interconnect. In this research, the surface roughness of the Cu thin film is controlled less than 2 nm in RMS by chemical mechanical planarization (CMP) process as shown in Fig. 2.

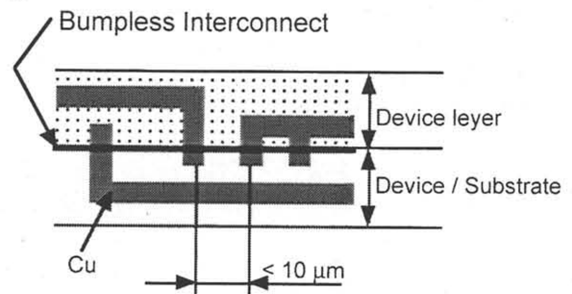


Fig. 1 Schematic representation of bumpless interconnects.

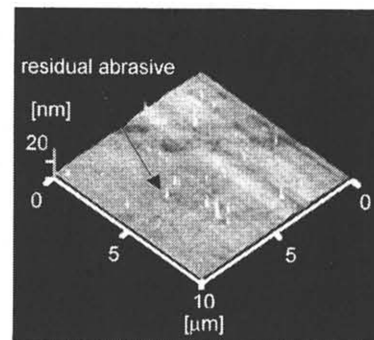
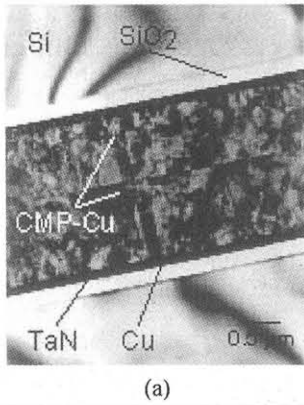


Fig. 2 AFM image of CMP-Cu surface.

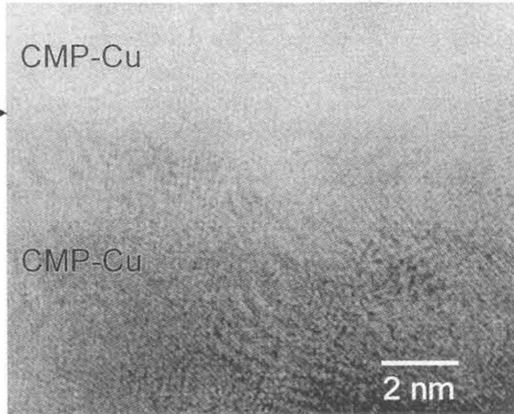
2. SAB for CMP-Cu Direct Bonding

To certify the feasibility of SAB for CMP-Cu direct bonding, the bonding experiments between simple CMP-Cu films were conducted.

Two CMP-Cu film samples were prepared on Si chips with different sizes of (20 x 20) mm^2 and (9 x 9) mm^2 after the deposition of SiO_2, TaN and Cu. Two surfaces are activated by FAB for 5 minutes under various vacuum pressures from 10^{-6} Pa to 10^{-3} Pa. Then the chips are pressed together under the contact load of 10 MPa. When the experiments are conducted in the better vacuum pressure than about 4 x 10^{-4} Pa, all pairs were successfully bonded at room temperature. After that the tensile test was carried out for bonded samples. All of the samples did not fracture at the interface between two Cu surfaces but in weaker materials. TEM images of the well-bonded interfaces are indicated in Fig. 3. Remarkable point here is that no voids and no intermediate layer can be seen at the interface and two surfaces are connected perfectly from the atomic view. It can be said from this result that SAB is highly beneficial method for CMP-Cu direct bonding.



(a)



(b)

Fig. 3 TEM images of the bonded interface of CMP-Cu: (a) whole image, (b) high resolutions image.

3. Fundamental Investigations on Bumpless Interconnect

Before going forward to the experiments on actual bumpless structure, electrical performances of CMP-Cu junction were observed. The test vehicle is consists of over 15000 microbumps in (4 x 4) mm^2 area, with the sizes of (10 x 10) μm^2 and the thickness of only 1 μm. The bump pitch is 10 μm and 24 pairs of them are wired to the electrodes for measurements of contact resistance. The bumps were interconnected to CMP-Cu plain film in the vacuum pressure of 10^{-5} Pa to 10^{-4} Pa. Most of the bumps were bonded successfully under the contact load of 0.64 g / bump as shown in Fig. 4. The contact resistance was less than 0.01 ohms and did not increase even after heated in the drying oven at 120 degrees for 500 hours. It can be said from this result that the electrical performance of CMP-Cu junction satisfies practical use.

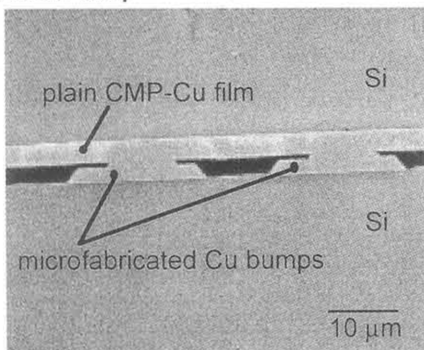
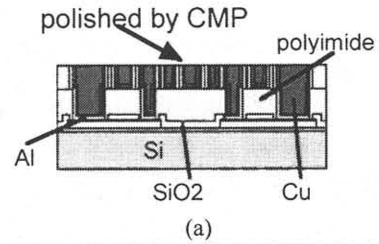
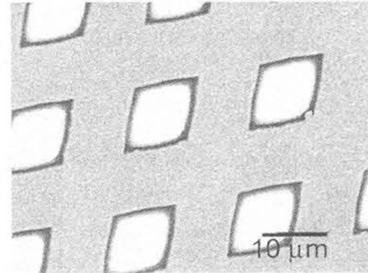


Fig. 4 The cross section image of bonded microbumps.



(a)



(b)

Fig. 5 The representation of the bumpless sample: (a) the construction, (b) SEM image of the sample.

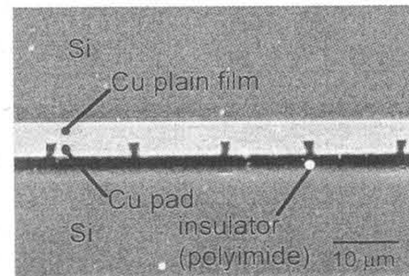


Fig. 6 Cross section image of bonded bumpless sample.

Finally, we conducted the bonding experiments on bumpless structure. Fig. 5 implies the construction of the sample. Cu contact pads of (10 x 10) μm^2 are placed at the same level as the insulators and bonded together to the simple CMP-Cu film. The pads were well interconnected as shown in Fig. 6 and did not fail at the interface.

4. Conclusions

We succeeded in direct bonding of CMP-Cu at room temperature using SAB method. Also, we showed that its high feasibility for ultra-high density interconnection, especially for bumpless interconnect.

Acknowledgements

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References

1. Rao R. Tummala, proc of the 3rd IEMT/IMC symposium, 1999, pp. 217-223.
2. T. Sakurai, proc of International Packaging Strategy Symposium, 2000, pp. 19-22
3. T. Itoh, T. Suga, proc of International Packaging Strategy Symposium, 2000, A-1-5.