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Characterization of Oxygen Vacancies in $SrTiO_3$ Thin Films by Auger Electron Spectroscopy and Its Application to Leakage Current Reduction of $Ru/SrTiO_3/Ru$ Capacitor

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1. Introduction

$SrTiO_3$ (STO) is a promising candidate as capacitor dielectrics in next generation DRAMs, because its dielectric constant is higher than that of SiO_2, SiN, and Ta_2O_5 [1]. One of the important issues for DRAM capacitors is leakage current reduction. The leakage current of STO capacitors is considered to strongly relate to oxygen vacancies in STO film. However, there was no convenient characterization method of oxygen vacancies in STO thin films.

In this paper, we characterized oxygen vacancies in STO films by Auger Electron Spectroscopy (AES) and applied to post-annealing study of Ru/STO/Ru capacitors.

2. Experimental

The 25nm-thick STO films were deposited by 2-step chemical vapor deposition (CVD) on ruthenium (Ru) bottom electrode. The detail of the 2-step CVD-STO described in previous report [1]. As a reference sample, sputtered $BaSrTiO_3$ (BST) film, which is same Ti contained oxide as STO, was used too. The samples were post-annealed between 250 and 600℃ in N_2 or O_2 atmosphere. I-V characteristics were measured for Ru/STO/Ru capacitors, in which Ru electrode was deposited by sputtering, by semiconductor parameter analyzer. AES spectra were measured by a conventional AES spectrometer.

3. Characterization of Oxygen Vacancies in STO Films by AES

It was reported that titanium oxidation states could be characterized in terms of Ti peaks in AES [2]. The Ti related peaks in AES were drastically changed by the oxidation states of titanium as shown in Fig.1 (a). The Ti LMV peaks split to two peaks [Fig.1 (b)]. The lower energy peak (~408eV), shown as O, was corresponding to Ti combined with oxygen. The higher energy peak (~415eV), shown as M, was corresponding to metallic Ti. The peak intensity ratios of O and M, denoted as AES M/O ratio, were 2.2, 0.5, and 0.22 for Ti_2O_3, TiO_2, $SrTiO_3$, respectively. The value of AES M/O ratio became smaller when the oxidation state of Ti was higher.

Figure 2 shows the typical I-V characteristics of Ru/STO/Ru capacitors. The I-V characteristics of CVD-STO sample were asymmetric, that is, the voltage range for relaxation current region with positive voltage bias was narrower than that with negative voltage bias. On the other hand, the sputtered BST sample showed symmetric I-V characteristics.

Figure 3 shows the in-depth profiles of AES M/O ratio. The AES M/O ratio near the bottom Ru electrode of the CVD-STO sample was high compared with the sputtered sample, indicating there was the layer with high oxygen vacancies in CVD-STO film near the bottom Ru electrode. For a sputtered sample, the low oxygen vacant layer (the layer with low AES M/O ratio) near the bottom Ru electrode was thicker than one of CVD-STO sample. It was found that there was a relationship between the symmetry in I-V characteristics and AES M/O ratio. The large value of AES M/O ratio indicated the existence of highly oxygen vacant layer, such as a conductive TiO and metallic Ti, and these conductive layers were considered to be a cause of narrow relaxation current region. Thus, it was found that the AES M/O ratio was very useful to characterize oxygen vacancies, which was a cause of high leakage current, in STO films.

4. Application to post-annealing of Ru/STO/Ru Capacitors

Figure 4 shows the post-annealing conditions for Ru/STO/Ru capacitors. The changes of AES M/O ratio at the bottom and top interface of STO film were shown as a function of annealing temperature in Figs. 5(a) and 5(b), respectively. The AES M/O ratio at the bottom interface increased gradually at high temperature. On the other hand, at the top interface, the ratio decreased with increasing of temperature. It wasn't possible for AES M/O ratio at both interfaces to reduce more than initial value by the 1step annealing. The typical I-V characteristics of post-annealed CVD-STO were shown in Fig.6. In case of 1step annealing sample, the relaxation current decreased with increasing of annealing temperature and the region of the relaxation current of positive bias was narrow for the increase of leakage current in high electric field region. Next, in case of 2step annealing sample, the oxygen vacancy at the bottom interface didn't increase as shown in Fig. 5(a) because of the oxygen annealing. But, the oxygen vacancy at the topside increased, therefore the leakage current increased in the 2step annealing condition as shown in Fig.6. The STO film followed by the 3step annealing had a good I-V characteristic as shown in Fig.6, because AES M/O ratio was smaller than initial value through the STO film. By the 1st 450℃(N_2) annealing, the oxygen vacancy in the STO film was most reduced using the excess oxygen in STO film, however the vacancy near the bottom interface could not be compensated as shown in Fig.5(a). Therefore, the 2nd 250℃(O_2) step needed due to supply the oxygen to the bottom interface. From these results, it was found that the high temperature annealing (3rd annealing) after the uniform compensation of the oxygen vacancy (1st and 2nd annealing) was effective for leakage current reduction of CVD-STO capacitors by monitoring AES M/O ratio.

5. Conclusion

Oxygen vacancies in STO films were characterized in terms of Ti peaks in AES. We found the clear relationship between peak intensity ration of metallic Ti to oxidized Ti and I-V characteristics. This technique was effectively applied to post-annealing study of Ru/STO/Ru capacitors. The characterization technique by AES is a powerful method to evaluate the oxygen vacancies in STO and other Ti contained oxide thin films.

Acknowledgements

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References

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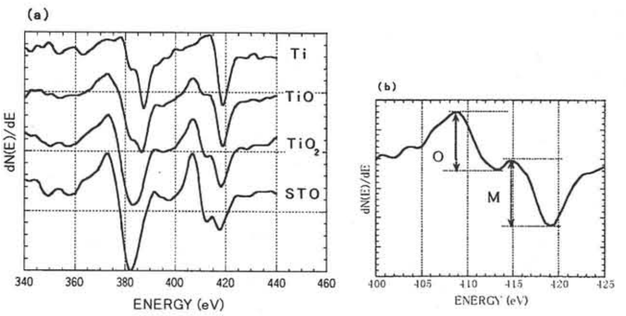


Fig.1. (a) AES line shape for titanium and its different oxides. (b) AES M/O ratio

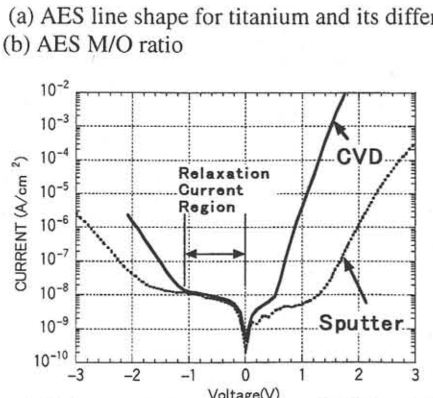


Fig.2. I-V characteristics of sputtered-BST and CVD-STO capacitors.

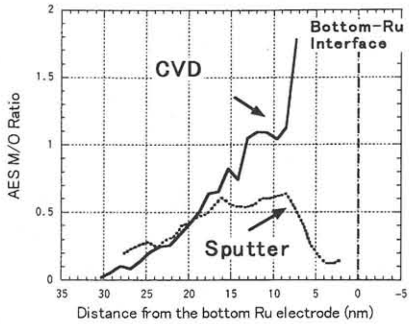
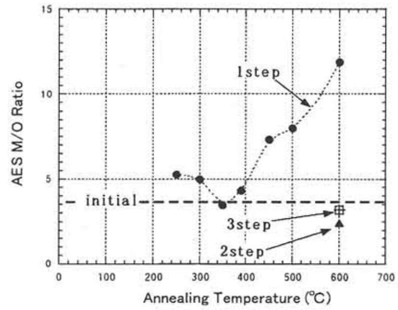


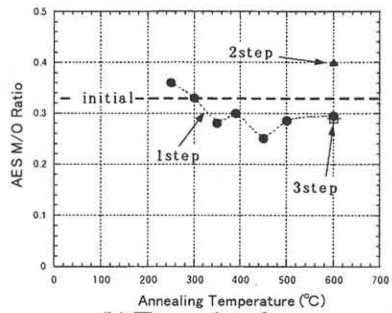
Fig.3. AES M/O ratio of sputtered-BST and CVD-STO capacitors

1step Annealing	*2step Annealing*	*3step Annealing*
250~600℃ (N_2) 60Pa 3min	250℃(O_2) 1atm 30min	450℃(N_2) 60Pa 3min
	↓ 600℃(N_2) 60Pa 3min	↓ 250℃(O_2) 1atm 30min
		↓ 600℃(N_2) 60Pa 3min

Fig.4. Annealing conditions



(a) The bottom interface



(b) The top interface

Fig.5. AES M/O ratio as a function of annealing temperature.

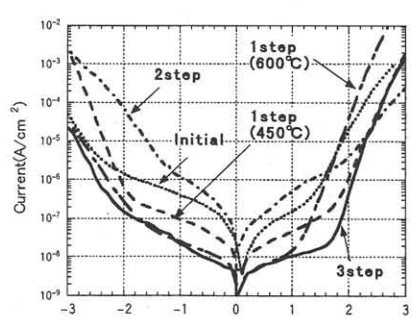


Fig.6. Annealing effect on I-V characteristic