Extended Abstracts of the 2001 International Conference on Solid State Devices and Materials, Tokyo, 2001, pp. 50–52

B-2-1 (Invited)

Recent Advances in SOP Integration

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1. Introduction: System-on-a-Package (SOP) Vision

The Packaging Research Center at Georgia Tech is working on novel System-on-a-Package (SOP) technology for next generation mixed-signal systems packaging. SOP represents a new paradigm in microelectronics packaging incorporating added functionality to the package, complementing the system-level integration on-chip. The PRC believes in a compeling need for converged and microminiaturized systems such as the wireless personal digital assistant (PDA) and network communicator that combine data, video, and voice. The PRC is currently working on the System-on-a-Package (SOP)-based Information Appliance (SOPIA) as a compelling system. Key enabled system attributes of the SOPIA include:

- Massively-parallel optical interconnects (allowing up to 16 Tbps performance);
- Reconfigurable wireless links (allowing up to 5 Gbps performance);
- High-performance computing (allowing up to 10 GHz processor speeds);
- Scaled down size (up to a factor 10-100X), and;
- Reduced cost, consistent with the market trend of a 10X decrease every two years.

The packaging technology enhancements include three parameters:

- I/O density at the IC-to-package interface, which drives I/O density to 3000 I/O/cm^2;
- Component density, which drives the embedded passives and optical waveguides and reduces the SOPIA size dramatically with upto 5000 components/cm^2; and
- Power or thermal density, which drives packaging for the SOPIA network communicator to achieve its ultra-high performance to 100 watts/cm^2.

At the heart of the new SOP strategy is a fully integrated substrate with ultra-high density wiring and integrated passive and optoelectronic components, and MEMS. The two major goals of this substrate technology are highest level of integration incorporating added functionality to the substrate; and lowest cost [1,2].

2. Organic Substrate Technology for SOP

The SOP technology at Georgia Tech is based on mixed-signal integration on low-cost organic substrate materials and processes. Traditionally, integration of RF/wireless, digital, and optical sub-systems have been accomplished on ceramic (LTCC) and inorganic (Si, Glass) substrate platforms. SOP and other emerging packaging technologies require very high wiring density. Such fine line signal conductors require low dielectric constant thin film materials. Organic /polymer dielectrics offer the benefits of low dielectric constant (ε_r = 2.0-4.0), leading to higher signal propagation speeds, as shown in Figure 1.

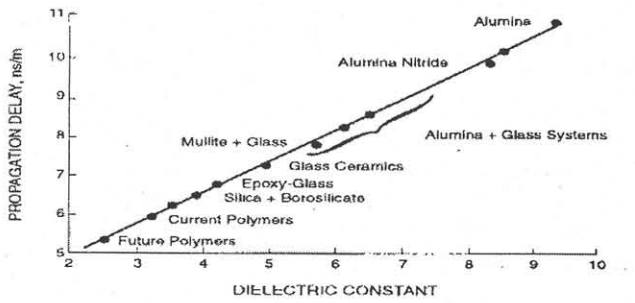


Figure 1. Propagation Delay vs. Dielectric Constant for Various Dielectric Materials[3].

The thinner films (10-50μm) used in new organic build-up technologies also offer the ability to design and implement ultra-high density wiring required to package emerging and future high I/O chip technologies. In most cases, organic technology also has the potential for reducing system packaging cost.

In the past, organic dielectrics have presented limitations due to higher loss tangent, high coefficient of thermal expansion (CTE), and low thermal conductivity. However, an emerging set of polymer dielectrics in sheet/film or liquid formulations offer a combination of very low loss and low CTE. Low loss polymers (tan δ < 0.002) like polyimide, poylphenyl ether (PPE), teflon etc. reduce heat generation in the substrate and reduce cross-talk, thus enabling signal traces to be spaced much closer. A summary of current and emerging organic materials and recent advances in SOP technology is presented in this paper.

3. Polymer/Organic Dielectrics for SOP

An integrated SOP substrate with embedded components and functions necessitates the use of both low and high dielectric constant materials. Polymers including PTFE, Polyimide, and Benzocyclobutene have been used in high frequency substrate applications because of their low ε_r and low loss tangent. These materials have found their niche applications, but cost is crucial for widespread acceptance of a material. Epoxy-glass laminate is the lowest cost material and consequently holds a large market share in package substrates and PWBs. But the relatively high loss tangent (0.015-0.025) of epoxy laminates and films limits their use to systems

operating below 2-3GHz. A new breed of polymer dielectrics are emerging to fill the gap between low-cost epoxy dielectrics and high-end, expensive materials like PTFE. These include polyphenyl ether (PPE) based materials, FR-4/PPO blends, liquid crystalline polymer (LCP), and lower cost PTFE and ceramic filled composites. Table 1 lists some common low dielectric polymers along with their dielectric properties at high frequencies. The R&D program at PRC is evaluating a number of these materials for use in mixed signal SOP applications at frequencies up to 20GHz and beyond.

Table 1. Common Low Dielectric Polymers and their Electrical Properties

Material	ε	Tan δ
PPE	2.9-3.2	0.001-0.002
LCP	2.8	0.002
Polyimide	2.9-3.5	0.002
Polyolefin	2.5	0.0005
BCB	2.9	<0.001

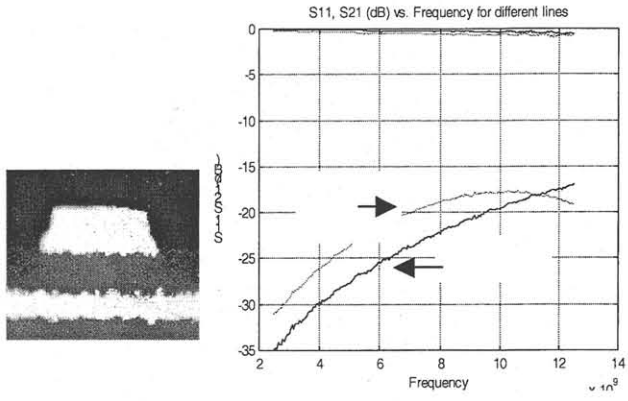
High dielectric constant materials are important for achieving high embedded capacitance in the substrate. This is particularly useful as mid-frequency decoupling capacitors for reducing ground bounce and simultaneous switching noise. Current surface mount discrete components will reach their limit of operation in the few hundred MHz range due to the high lead inductance associated with solder interconnects. Novel polymer-ceramic nanocomposite dielectric materials have been developed at the PRC for embedded capacitors and ε_r of 100-150 has been recently demonstrated. These materials are also being explored for tunable capacitors as MEMS components.

4. Recent SOP Accomplishments at PRC

PRC's process integration research involves a number of unique testbeds that bring together the entire gamut of PRC research innovations into technology demonstration platforms. A brief summary of recent SOP adva nces at the PRC is shown below.

- *Characterization of Thin Film Polymer Dielectrics up to 10GHz.*

It is critical to accurately characterize the dielectric constant and loss tangent of the dielectric materials prior to using them in high frequency designs. Recently, a new low-loss resin coated copper (RCC) dielectric was characterized upto 6 GHz using a hybrid coplanar waveguide-microstrip (CPWM) structure. Standard SOLT calibration was performed and the effective dielectric constant (ε_{eff}) was extracted from the measured S_{11} and S_{21} data. Ansoft simulations were used to derive the dielectric constant of the material. DC capacitance measurement was used to obtain ε_r at low frequency. The dielectric constant was calculated to be 3.48 at DC, 3.45 at 1GHz, and 3.28 at 6 GHz. This correlates well with the vendor supplied data which was measured at discrete frequencies using resonators. An attenuation of 1.2 dB/cm was achieved at 6 GHz which compares well with the performance of other dielectric materials being used in high frequency applications. Figure 2a shows a cross-section of the signal line and Figure 2b shows the measured S-parameters from two different line lengths.



- *High-Q Embedded Inductors for Wireless Applications*

Embedded inductors with high quality factors have recently been demonstrated within the high density wiring scheme of SOP substrates[4,5]. The substrate was lossy FR-5 having a tanδ=0.009 and ε_r=3.7 at 1GHz. The thin film epoxy dielectric had a tanδ=0.015 and ε_r=3.4 at 1GHz. Cascaded loop microstrip inductors and coplanar waveguide (CPW) loop inductors were designed on laminate and build-up dielectric materials. A ground plane separation of approximately 42 mils was used, which is well suited for planar microstrip inductors. The CPW inductors were fabricated on the laminate substrate using conventional PW etching processes. Table 2 summarizes the measured data for the various inductors. Measurements were made with a 1-port network analyzer(VNA) after SOLT calibration. A point worth mentioning is that the size of the inductors compares well with the inductors in LTCC technology with similar performances [6].

Table 2. Tabulated data for Microstrip & CPW Loop Inductors

Type	Qmax	L(nH)	SRF (GHz)
1 loop microstrip	103 at 2.2 GHz	11nH at 2.2GHz	3.6
2 loop microstrip	38 at 1.2 GHz	20.5nH at 1.2GHz	2.2
3 loop microstrip	23 at 0.65 GHz	29nH at 0.65 GHz	1.6
CPW Loop 3mil Line	75 at 5 GHz	2nH at 5GHz	~11
CPW Loop 5mil Line	85 at 5 GHz	1.85nH at 5GHz	~11

- *Fine Line High Density Wiring*

PRC has demonstrated ultra-fine line structures on large area SOP organic substrates using low-cost processes. Line

widths of 15-25 μm and microvia interconnects with diameters of 25-100 μm have been achieved. Figure 3 shows a comb structure having 15 μm ultra-fine lines on 12"x12" SOP-3A testbed FR-5 substrate.

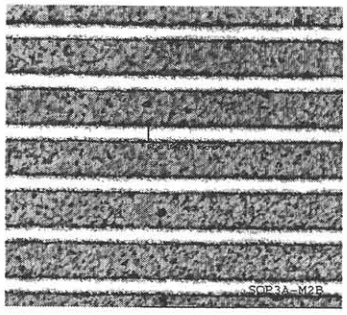


Figure 3. Micro photograph of plated 15 μm copper lines on 40 μm pitch on build-up layer of SOP-3A 12"x12" substrate.

Reliability of the microvia interconnects on SOP substrates is critical to the realization of high density package wiring. Recent studies indicate that vias down to 25μm diameter passed 2000 liquid-to-liquid thermal shock cycles of testing between -55°C and 125°C. The average initial resistance of a 50 μm microvia was measured to be around 1 mΩ. A cross-section of a 75μm microvia after thermal shock testing is shown in Figure 4.

Summary

The PRC has made significant strides in the development and characterization of its System on a Package concept for next generation microsystems, such as Information Appliances. Embedded R, L, and C's have been demonstrated along with a highly reliable high density interconnect technology on large area substrates. The test beds that have been put in place will allow the Center to evaluate many of the other critical technologies that are required to support SOP, such as embedded optics and MEMS, mixed signal test, module assembly and thermal cooling methodologies.

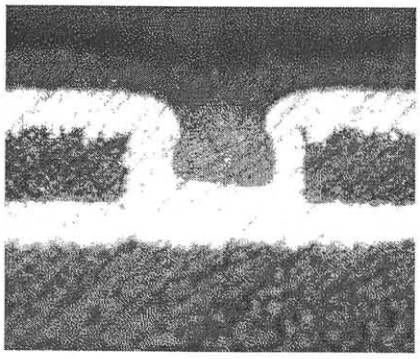


Figure 4. Cross-section photograph of a 75 μm microvia that survived 2000 thermal shock cycles

Acknowledgment

This work was supported by the National Science Foundation through the Georgia Institute of Technology/NSF Engineering Research Center in Electronic Packaging (EEC-9402723). The authors would like to thank all the SOP team members including design, fabrication and test researchers, faculty and students.

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