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Interconnect Length Distribution in Si System ULSI

Naohiro Takagi, Hiyouko Shinoki, Tomohito Tsushima, Yoshisato Yokoyama and Kazuya Masu

Precision and Intelligence Laboratory, Tokyo Institute of Technology
Nagatsuda 4259, Midori-ku, Yokohama, 226-8502, Japan

1. Introduction

Distribution of interconnect length in ULSI chip is significant for evaluating future ULSI performance such as speed and power consumption. Based on Rent's empirical rule, the interconnect length distribution is derived for the chip that has unique Rent's parameter set of k and p. However, realistic ULS chips have various kinds of circuit blocks such as logic and memory.

In this paper, we derived the interconnect length distribution introducing the averaging method in counting the number of interconnect of chip that have different function circuit blocks. From the computer simulation results, it is demonstrated that, in memory-logic LSI, memory bock that has small value of p should be placed at the corner of the chip to reduce the number of long interconnect.

2. Deviation of the Interconnect Length

Figure 1 shows the Rent's empirical rule of various kinds of ULSI chip; $N_p = k\,N_g^{\,p}$, where N_p is the number of external pins, N_g the number of gates or bits, k and p Rent's empirical parameters. The logic circuit has relatively large p and small k value, and the memory has small p and large k values, respectively. We assume that the chip is divided into 2 circuit areas of **Area-1** and **Area-2** whose numbers of gates are N_1 and N_2, respectively, and that **Area-1** is placed at the corner of the chip as shown in Fig. 2(b). When (1) **Block-A** is in **Area-1** and (2) **Block-B** is spread in **Area-1** and **Area-2** as shown in Fig. 3, the number of interconnects is calculated by averaging depending on the area which occupies **Area-1** or **Area-2** as indicated in the equation below. According to this deviation, computer simulation algorithm can be performed.

3. Results and Discussion

Figure 4 shows the interconnect length distribution of the chip that has unique Rent's parameter set of k and p. Chip with large p value such as logic chips has more long interconnect.

Figures 5, 6, and 7 shows the interconnect length distribution of the chip has multi functions of memory and logic. In Fig. 5, the memory block that has small p value is placed at the corner. In this case, the number of relatively long wire reduced. On the other hand, the logic block is placed at the corner as shown in Figs. 6 and 7, the number of long wire is increased as compared with the chip in which the entire circuit block is composed by logic. This is because a logic block has large number of output interconnect to outer area of the logic block. The above results show that in logic and memory mixed LSI, placing the memory block at the corner of the chip as shown in Fig. 5 is desirable to reduce the number of long interconnects.

4. Summary

We have derived the interconnect length distribution of the chip which has different circuit functions. Computer simulation results have shown that, when the circuit such as memory is placed at the corner, the number of long wire is reduced.

References

[1] J. A. Davis, et al, IEEE **ED-45**(3), 580 and 590 (1998).

[2] H. B. Bakoglu, "*Circuits, Interconnections, and Packaging for VLSI*", Addison-Wesley, 1990.

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When **Block-A** is in **Area-1** of Fig. 2(b), the number of interconnects that has a gate length l is given by

$$i(\ell) = \sum_{i=1}^{\sqrt{N_1}} \sum_{j=1}^{\sqrt{N_1}} \left[\begin{array}{l} \dfrac{(N_{A1}+N_{B1})\alpha_1 k_1 (N_A+N_B)^{p1} + (N_{A2}+N_{B2})\alpha_2 k_2 (N_A+N_B)^{p2}}{N_A+N_B} \\ -\dfrac{(N_{B1})\alpha_1 k_1 (N_B)^{p1} + (N_{B2}) k_2 (N_B)^{p2}}{N_B} + \dfrac{(N_{B1}+N_{C1})\, k_1 (N_B+N_C)^{p1} + (N_{B2}+N_{C2})\alpha_2 k_2 (N_B+N_C)^{p2}}{N_A+N_B} \\ -\dfrac{(N_{A1}+N_{B1}+N_{C1})\,\alpha_1 k_1 (N_A+N_B+N_C)^{p1} + (N_{A2}+N_{B2}+N_{C2})\alpha_2\, k_2 (N_A+N_B+N_C)^{p2}}{N_A+N_B+N_C} \end{array} \right]$$

where $N_{A1} = 1$, $N_{A2} = 0$, $N_{A1} + N_{A2} = 0$, $N_B = N_{B1} + N_{B2}$, and $N_C = N_{C1} + N_{C2}$. $\alpha_1 = fo^1/(fo^1+1)$ *and* $\alpha_1 = fo^2/(fo^2+1)$, where fo^i (i = 1 and 2) is average fun-out of the gats in **Area-*i***.

If the chip has unique k and p values, $N_{B1} = 0$, and $N_{C2} = 0$, and the above equation is reduced to Eq. (A16) of Ref. 1.

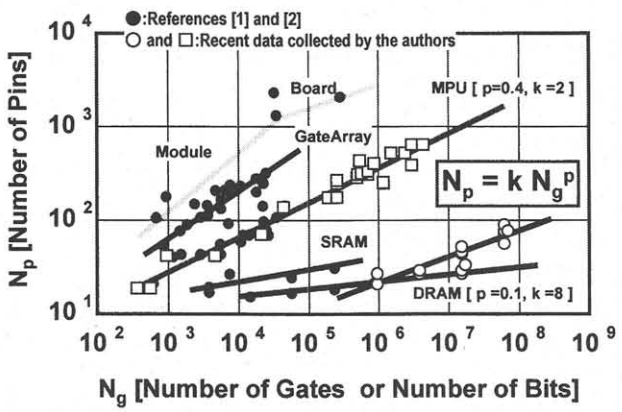

Fig. 1 Number of external chip terminals as a function of number of gates or bits.

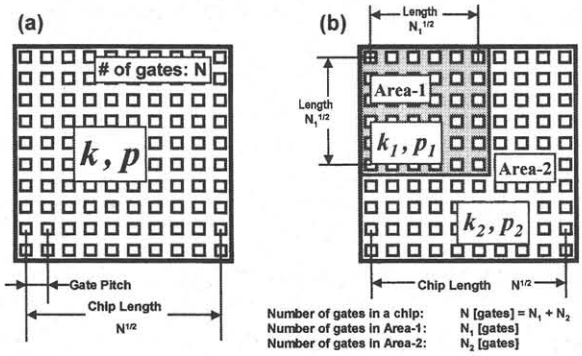

Fig. 2 Number of external chip terminals as a function of number of gates or bits.

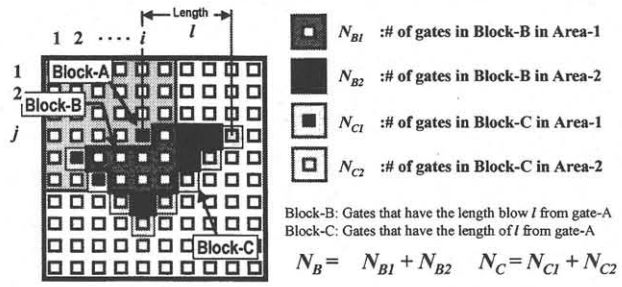

Fig. 3 Wire length calculation method.

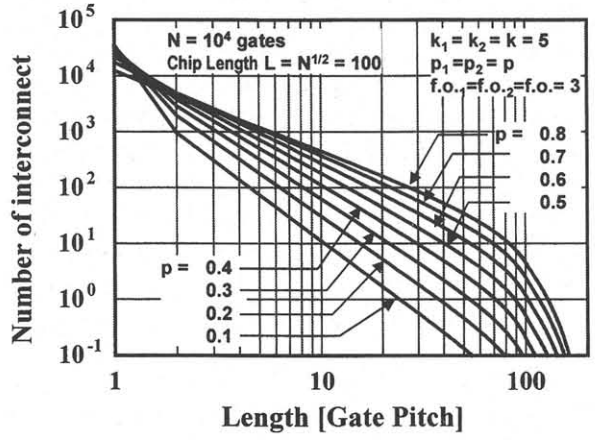

Fig. 4 Interconnect length distribution: single function chip.

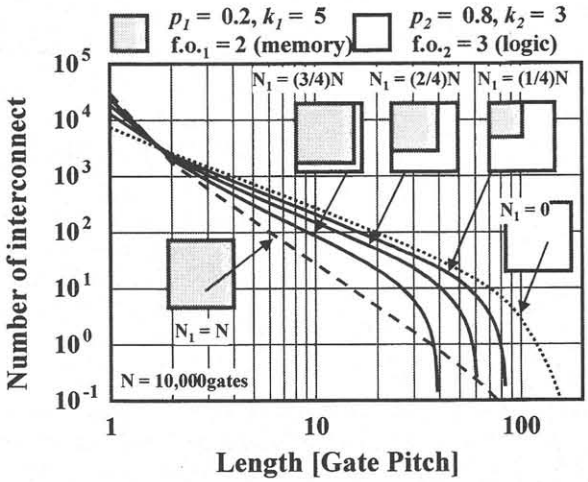

Fig. 5 Interconnect length distribution: multi function chip.

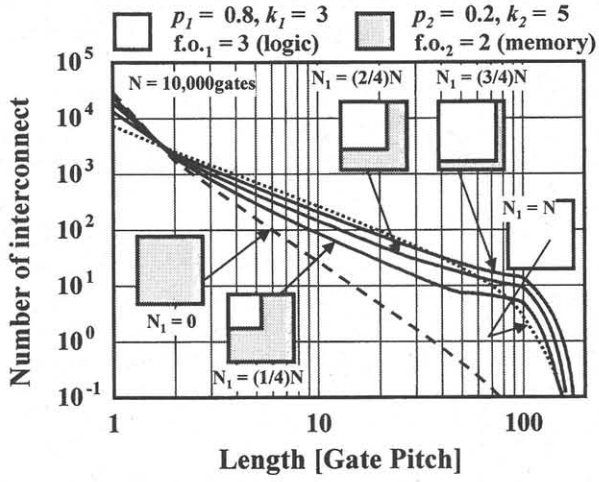

Fig. 6 Interconnect length distribution: multi function chip

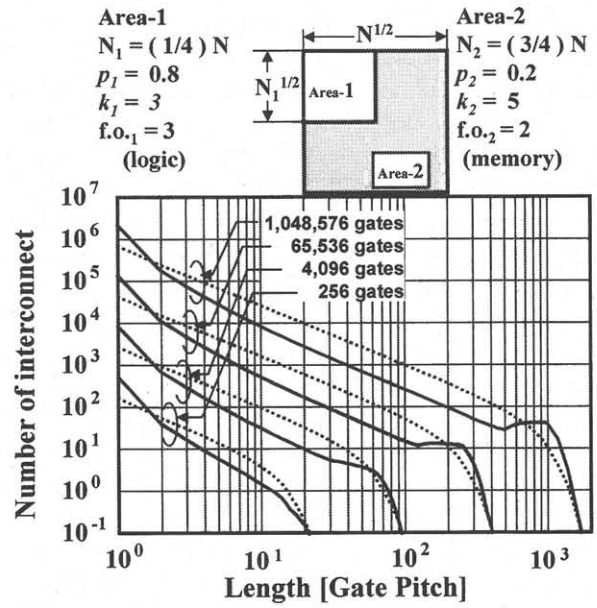

Fig. 7 Interconnect length distribution: multi function chip